Overcoming Mechanical Drilling and Registration for High Layer Count RF and Digital PWBs Containing PTFE

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PTFE containing composites offer the promise of exceptional electrical benefits at high frequency. However, this attraction to PTFE is soured by some manufacturers' vision of the fabrication challenges of PTFE. Mechanical drilling and registration are two key areas in which many fabricators struggle at high layer counts. This learning curve hurdle can be greatly reduced by understanding some key processing variables. Recent introductions of non-reinforced PTFE prepregs and dimensionally stable cores offer the promise of building 250-300 mil large format PWBs in the same quality and predictability as FR-4. However, the attractiveness of isotropic, electrically homogeneous fiberglass-free dielectrics is diminished by some fabricators' lack of experience in fabricating PWBs containing PTFE and little or no fiberglass.

While fiberglass rich PTFE composites might be more dimensionally stable, fiberglass suffers from the following drawbacks:

(1) High 0.0067 DF at 10 GHz that becomes increasingly worse with frequency
(2) Fiberglass is very anisotropic at the millimeter/micron level.

Publications highlighting the drawbacks of using fiberglass based laminates in multilayer stripline applications are numerous. Various authors have shown the high level of impedance variation that can be observed by TDR as a transmission line crosses between the windows and knuckles of woven fiberglass[1]. Loyer has shown that while there might be an average skew number depending on how the transmission lines are routed on a typical FR-4 based PWB, there is a distribution of skew that will occur on a fiberglass reinforced FR-4 composite such that some transmission lines can be much better or worse than others[2]. The ideal case is a fiberglass poor stripline structure. A PWB with excellent electrical properties that cannot be manufactured in yield and with predictability is of no use to the industry.

This publication will:

(1) Suggest to fabricators how to effectively mechanically drill high layer count multilayer PWBs containing PTFE and discuss the problem of drill wander on registration

(2) Briefly describe the electrical properties of a non reinforced prepreg tested in an ATE application at 12 gbps. The non-reinforced prepreg is shown in Figure 1 bonding together a top and bottom layer core of FR-4, the FR-4 being included for contrast only to highlight the difference between a fiberglass reinforced core that is fairly common in the industry and a non-reinforced prepreg that is somewhat new to this industry.

Designers generally accept the claims of the exceptional electrical properties of ceramics like silica and thermoplastics like PTFE. A great deal of emphasis during the β-testing of a series of PTFE containing prepregs and cores focused on working with high volume, large format backpanel manufacturers to understand the mechanical drilling of composites containing some level of PTFE. The goal was to improve the quality of the drilled hole wall particularly with respect to plating nodules. Some OEMs have 1-2 mil nodule specifications while others see any nodules as a potential risk to long term reliability. While not all PWB applications have the concern that a plating nodule might damage a press fit connector, the plating of poorly drilled via structures can lead to shorts or opens. In digital applications at high frequency the vias and ground vias are highly tuned with respect to capacitance/inductance so that the via itself provides a smooth 50 ohm or 100 ohm transition without a high level of return loss/insertion loss roll off. In a microwave application one worries that copper plated debris in a through hole can significantly degrade filter or coupler performance. The installed FR-4 base of fabricators and suppliers has experience drilling FR-4 and optimized their processes around FR-4. Today's ceramic loaded PTFE composites have been optimized for reduced expansion/contraction and insensitivity of DK and DF to temperature, frequency, and moisture. Although improvements have been made to PTFE containing composites yielding more homogeneous composites that are easier to drill and plate, a fabricator has to take the time to understand what is being fabricated.

First a basic strategy to mechanically drill standard ceramic loaded PTFE laminates will be presented. Figure 2 shows a photomicrograph of a cleanly drilled multilayer PWB. Figure 3 shows what looks to be PTFE hairs attached to an interconnect pad. This defect is a common problem encountered by fabricators and often leads to plating nodules. Secondly, the defect raises questions about long term reliability. An 18 layer, 165 mil backpanel sized board produced with one oz. copper was cross sectioned, carbon coated, and analyzed using a JEOL 5300 Scanning Electron Microscope using voltages of 20-25 kV in combination with a Kevex SiLi detector that used backscattered electrons in either the compositional or topographical models. Typically copper generates a series of **three** KeV peaks. Because an electron beam causes a cascading effect of excited secondary electrons and x-rays, 4-6 microns is the typical beam resolution. Therefore, neighboring copper is typically included in many EDX scans. SEM/EDX was used to analyze a plating nodule occurring at an interconnect pad. Figure 4 is interesting because the low energy copper KeV peak has disappeared in the EDX scan. The electron beam was focused directly into the black area in Figure 4. This suggests that the low energy back scattered copper electrons have disappeared which is consistent with focusing the electron beam into a deep void. Figures 3 and 4 combined with exhaustive analysis of similar defects strongly suggests that the "hairs" are actually voids. What, then, is the source of these voids?

18 layer PCB samples were potted, after which the plated copper was etched out of the sidewall leaving the bare hole wall, associated debris, and the potting compound

still in place. Figure 5 shows the multilayer PWB after the through hole was sectioned and the plating removed. The interconnect pad can also be seen to have been removed during etching. Directly above where the interconnect pad used to be is a loose collection of bound particles. EDX shows PTFE, titanium dioxide, and silica. The fact that the loosely associated group of particles rests just above the interconnect pad strongly suggests that the dominant mechanism causing these defects is the interconnect pad scraping drill bit debris off the bit as the bit enters and exits. After thoroughly analyzing other areas showing the same defect as Figures 3 and 4, the evidence is compelling that the mechanism resulting in these hair-like voids and nodules is debris that builds up onto the drill bit and scrapes off onto the sidewall when the bit hits a copper interconnect pad. This loosely associated lint-like collection of particulate then challenges the plating process. Electroless and electrolyzed plating chemistry try to plate in and around the random collection of debris that is attached to the side wall leaving plating voids.

Drilling is a dynamic process. Material is reduced in size to particulates with the hope that the debris moves up the flutes and is evacuated by the vacuum system. Figure 6 shows an SEM scan of a sidewall where no defects can be observed. However, drill bit debris can be seen lining the sides of the hole walls. When one uses scanning electron microscopy to look very closely at hundreds of holes after etching away the copper, one is likely to see defects that are normally plated over and embedded into the copper. Figure 7 shows a good via versus a bad via before plating. High pressure washing may loosen attached debris from the hole walls but it won’t remove debris that is fused to the sidewall by hot PTFE.

There are many variables when drilling printed circuit boards including entry materials, exit materials, drill rpm, infeeds, chip loads, hit count, primary angle of the drill bit, drill type, retract rate, etc. The secret of drilling PTFE is not to allow debris to build up on the surface of the drill bit. PTFE is a soft material; as PTFE gets hot it acts as a binder and will glue the debris to the flutes of the bit. As the drill bit burrows the hole, it strikes the copper interconnect pad and debris scrapes off the bit, leaving debris deposited on the interconnect pad. Drill bit debris cannot be allowed to build up on the bit but how do you accomplish this?

The key variables include:

(1) PTFE should be drilled with a low chip load and low speeds, a chip load around 1 depending on bit diameter, as low as 0.5 preferred for small diameter holes
(2) PTFE should be drilled with a thick, hard phenolic entry material
(3) Dwell time between hits is beneficial in allowing the drill bit to cool.

Figure 8 shows the condition of a drill bit inundated with debris. Good drilling parameters should allow no debris to accumulate in the flutes of the bit. Drill bit debris can be removed from the bit by drilling the contaminated bit into a hard material like phenolic. The objective is to abrade the drill bit debris onto the hard sacrificial entry material. One DOE began by drilling twenty 0.0028” holes into a 200 mil thick ceramic filled PTFE multilayer PWB (Figure 9a, left). The PWB was removed from the drill table and replaced by a 160 mil slab of phenolic. Drill bits full of debris were drilled 20 hits into the phenolic and examined thereafter (Figure 9a, right). The hard phenolic effectively abraded the debris off the drill bit, cleaning the bit. The drill bits were alternately drilled 20 hits into the PCB, 20 hits into the phenolic, reaching 200 hits into the PCB and 200 hits into the phenolic. Figure 9b (left), for example, shows the drill bit fairly coated with PTFE debris from hits 80 to 100 and a loosely attached hanging thread. Hits 80-100 into the phenolic (Figure 9b, right) effectively cleaned the drill bit. This experiment demonstrated that through 200 hits, the drill bit could be effectively cleaned from PTFE debris by using hard phenolic to abrade the PTFE off onto the phenolic. Although phenolic may not be the best entry material, phenolic performed better than using FR-4 as an entry material. It is postulated that a harder phenolic may work better.

However, removing a backpanel sized PCB from the drill table and alternating with a phenolic dummy every twenty hits is not a practical manufacturing solution. The next experiment used a thick piece of phenolic as the entry material to essentially clean the drill bit every hit as opposed to waiting for 20 hits and allowing drill bit debris to build up on the bit. The largest unknown was how thick the phenolic entry should be to effectively abrade all of the debris off the drill bit before it began to drill into the 200 mil thick ceramic filled PTFE PWB. A 200 mil thick 20 layer ceramic filled PTFE based PWB was drilled with the following parameters: 32K speed, 48K infeed, chip load = 1.5, 1 second dwell between hits, 28 mil diameter straight shank Kemmer bit, retract rate 1000, 70 mil phenolic exit material. The entry and exit materials are summarized in Table 1.

Table 1

Trial	Entry 1	Entry 2	Increasing peck depth (mil)	Sectioned PTHs	% PTHs having >1.4 mil nodules	Visual Observations
1	48 mil phenolic	no	no	30	17	
2	15 mil Al clad phenolic	48 mil phenolic	no	27	41	flute totally blinded
3	15 mil Al clad phenolic	48 mil phenolic	no	26	19	
4	15 mil Al clad phenolic	48 mil phenolic	no	27	41	
5	15 mil Al clad phenolic	94 mil phenolic	no	27	41	flute totally blinded
6	15 mil Al clad phenolic	94 mil phenolic	no	26	46	flute totally blinded
7	140 mil phenolic	15 mil Al clad phenolic	no	25	-	hole plugs
8	140 mil phenolic	15 mil Al clad phenolic	no	27	-	hole plugs, flutes plugged
Trials 1-8 all suffered from a poor evacuation of debris						
9	15 mil Al clad phenolic	48 mil phenolic	71, 55, 55, bottom	57	14	debris coating on bit easily removed by hand
10	15 mil Al clad phenolic	94 mil phenolic	71, 55, 55, bottom	55	44	large piece of phenolic at tip of bit
11	15 mil Al clad phenolic	140 mil phenolic	75, 75, 55, bott	54	35	beautiful looking bit
12	15 mil Al clad phenolic	48 mil phenolic	65, 55, 55, bottom	72	6	phenolic piece on tip of bit
13	15 mil Al clad phenolic	94 mil phenolic	55, 60, 55, bottom	72	15	very clean drill bit
14	15 mil Al clad phenolic	140 mil phenolic	75, 75, bottom	73	12	1 plugged hole

Trials 1-14 show the use of various thicknesses of phenolic entry material to essentially abrade the PTFE debris from the bit before it could drill into the PTFE based PWB. 48 mil, 94 mil, and 140 mil phenolic entry material was used. Trials 1-8 highlight the use of thick phenolic entry with no peck drilling. The problem with using thick phenolic entry material is the difficulty in evacuating all the phenolic debris which is a new variable. Trials 5-8 using 94 mil and 140 mil phenolic entry resulted in drill bits and hole plugs inundated with phenolic. In the absence of peck drilling, only trials 1-4 had some hope of success using the thinner 48 mil thick phenolic. Trials 9-14 took advantage of peck drilling to remove debris more effectively. As shown in Table 1, the trials using the 48 mil phenolic entry outperformed the trials using the 94 and 140 mil thick phenolic entry.

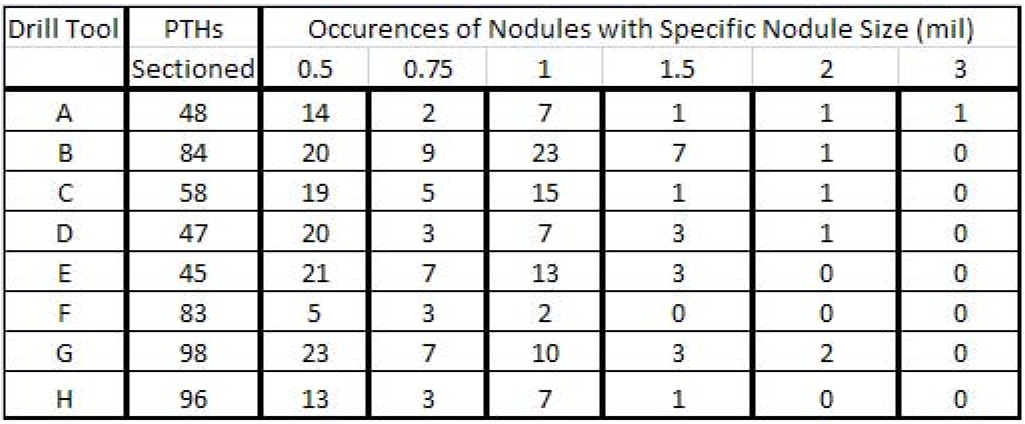
Although the thicker phenolic entry is more effective at cleaning the PTFE based debris off the bit, the phenolic entry itself becomes difficult to remove during drilling. Trials 9 and 12 are interesting because they use the same drill conditions with the only modification being the peck depth. Trial 12 yielded the best results from Table 1 when the first peck drilled to a depth of 65 mils (48 mil phenolic + 15 mil Al clad phenolic) effectively only traveling to the depth of the phenolic to clean the bit, then retracting to remove debris associated with the phenolic. This yields a penetration of only 1-2 mils into the PCB before the phenolic debris is evacuated and the cleaned drill bit is free to start drilling a single hole in the PCB. In trial 12, the first peck traveled 65 mils, barely passing beyond the entry materials into the PCB, the second peck drilled an additional 55 mils (total depth of 120 mils) before retracting, the 3rd peck an additional 55 mils (175 mil depth), the final peck drilling to the bottom of the PCB.

It should become obvious to the reader that there are a lot of variables to mechanical drilling. Future experiments should focus on the optimum thickness of phenolic entry to balance cleaning the drill bit and evacuation of the phenolic, the hardness of phenolic, and optimum pecking.

Another variable investigated was the dwell time between hits. A dwell time between hits is used conceptually to allow the drill bit to cool. Normally PWB fabricators drill at the maximum possible speeds to achieve the highest possible utilization of the drill machines using nanosecond dwell times between hits. A similar experiment was conducted with a standard 10 mil phenolic entry material to look at the dwell times between hits. The following dwell times were used between hits 0.04, 1, 2, 3, 4, and 8 seconds. No peck drilling was used. The short conclusion is that the trial with a dwell time of 0.04 seconds between hits had 3x the nodules of the trials using 1-8 seconds. There was no apparent advantage in using longer than 1 second. This experiment was conducted prior to the DOE conducted in Table 1 so it is quite possible that the peck drilling may be sufficient to allow the drill bit to cool without a dwell time between hits. One second dwell might also prove no better than 0.5 seconds or 0.25 seconds.

A further study was conducted specifically on 10 mil drilled holes to compare the drill quality of different drill geometries. The smaller 8, 10, 12 mil drill bits raise the level of complexity. Small drill bits are more prone to breakage and they are much more susceptible to drill wander. Because small drill bits are more prone to breakage, one has to balance the thickness of the phenolic entry versus the increased level of breakage that occurs with a longer fragile drill bit. Small drill bits will deflect off hard materials in the composite causing wander. Drill wander is another level of complexity that challenges registration of innerlayers above and beyond the dimensional stability of the innerlayers during fabrication. The following drill parameters were used and all held constant: entry material (7 mil Al, 16.5 mil phenolic entry) exit material (16.5 mil phenolic), infeed (55 ipm), speed (120K rpm). This set of drill conditions was found previously to be a solid set of drill parameters for 10 mil holes. Four vendors of drill bits were evaluated. Both undercut and straight shank bits with various helix angles were evaluated. Typically thicker phenolic entry would be preferred for better removal of debris from the drill bits. Regrettably, not all vendors could supply drill tools of sufficient length to allow for thicker phenolic entry material. The ceramic filled PTFE substrate material was approximately 115 mils thick and had 1 oz copper planes every 10 mils. The drilled holes were then visually evaluated before plating, metalized, and reevaluated by tedious cross sectioning. Nodules in the plated through holes (PTHs) were counted and ascribed to a certain size (mil) so that a size distribution of plated nodules could be obtained. The plated nodule size distribution is summarized in Table 2.

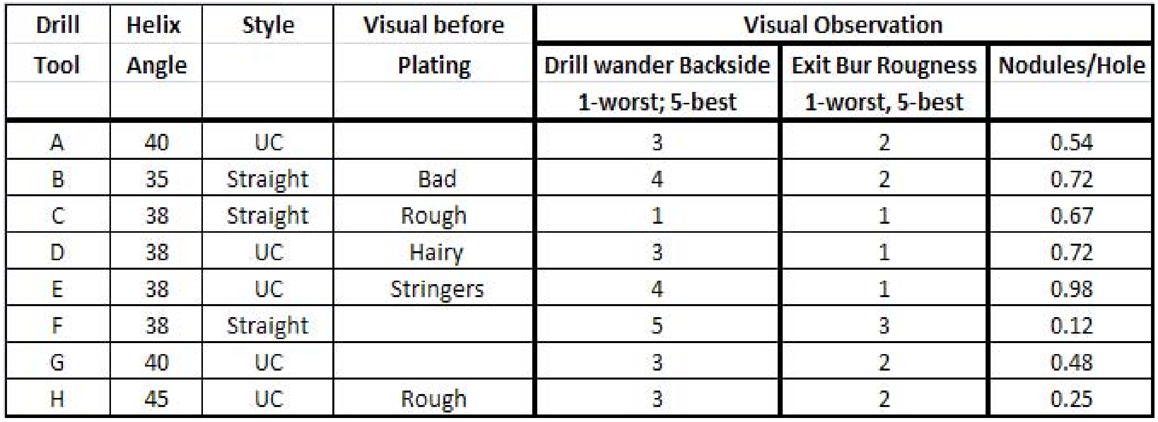
Table 2



Drill Tool	PTHs	Occurences of Nodules with Specific Nodule Size (mil)					
	Sectioned	0.5	0.75	1	1.5	2	3
A	48	14	2	7	1	1	1
B	84	20	9	23	7	1	0
C	58	19	5	15	1	1	0
D	47	20	3	7	3	1	0
E	45	21	7	13	3	0	0
F	83	5	3	2	0	0	0
G	98	23	7	10	3	2	0
H	96	13	3	7	1	0	0

From this crude analysis Drill Tools F and H showed the least amount of plating nodules and the smallest number of large nodules relative to the number of 10 mil holes cross sectioned. The drill geometries are summarized in Table 3. Table 3 contains a category listed as the number of nodules divided by the 10 mils cross-sectioned in attempt to attach a score to the relative roughness of the hole corresponding to each drilling condition. From this scoring, drill tools F and H showed the best results.

Table 3



Drill Tool	Helix Angle	Style	Visual before Plating	Visual Observation		
				Drill wander Backside 1-worst; 5-best	Exit Bur Rougness 1-worst, 5-best	Nodules/Hole
A	40	UC		3	2	0.54
B	35	Straight	Bad	4	2	0.72
C	38	Straight	Rough	1	1	0.67
D	38	UC	Hairy	3	1	0.72
E	38	UC	Stringers	4	1	0.98
F	38	Straight		5	3	0.12
G	40	UC		3	2	0.48
H	45	UC	Rough	3	2	0.25

Drill tool F was a straight shank tool. Drill Tool H was an undercut bit with an unusual 45° helix angle. Contrary to popular thought, undercut bits did not show any advantages versus a straight shank tool using this set of drilling conditions. A standard straight shank drill tool outperformed all candidates. In fact, drill tools E and F were from the same vendor, with this vendor's undercut tool being the worst candidate and their straight shank tool being the best. . Figure 10 shows good and bad examples of the quality of the plated through holes.

The backside of the test substrate was also evaluated visually for drill wander. Generally speaking, the best drill parameters may not correspond to the least amount of drill wander so a set of drill conditions must be adopted that balances an acceptable level of drill wander with acceptable hole wall quality. Small diameter drill bits are particularly prone to wander when drilling high aspect ratio through holes. Again drill tool F outperformed the other drill geometries, having the least amount of drill wander. Figure 11 shows an example of drill wander observed from the top and backside of drilled 10 mil holes. Because the drill parameters were fairly well optimized, the drill bits showed no sign of the flutes being filled with debris. Drill bits that have flutes full of PTFE and related debris are even worse from a drill wander perspective. Figure 12 shows the related impact on registration caused by drill wander. The drilled holes are not centered in the circular pad. Figure 12 is also noteworthy due to the lack of fiberglass in the cross section. With good processing parameters, 20-30 layer, 150-275 mil thick multilayers are being fabricated in a predictable fashion with virtually no fiberglass reinforcement.

Many people understand that high quality PTHs are preferred from a reliability viewpoint. However, for microwave designs where designers are embedding filters or couplers inside a PWB, through hole quality is essential. If a PTH is used in the design of filters or couplers and random debris occurs on the interconnect pad, this has the possibility of influencing the capacitance/inductance of the circuit and being detrimental to the performance of the filter/coupler. Poor registration can also affect the performance of a filter embedded in a multilayer design. Registration is a challenge that has its roots in the performance of the core materials. If a core material is poor at maintaining registration, then the problem is exacerbated by drill wander of the tool. Taken together, registration and plating debris (nodules) are serious problems for the filter and coupler designer.

The digital designer has the further challenge that state of the art designs are moving to pitch. 0.4 mm and 0.5 mm pitch are becoming standard in the semiconductor test area. This trend corresponds to the use of smaller drill bits. The trend in microprocessors is to higher I/O count meaning there is a pressure on densification in the semiconductor test area. Thousands of I/Os make it essential that the PWB supplier takes the time to understand all of the factors that lead to poor drilling and poor registration.

<u>Electrical Properties</u>

Now that is has been established that high layer count PWBs containing PTFE can be fabricated, the electrical properties of the non reinforced silica loaded prepreg combined with a high performance core will be described. This non reinforced prepreg has a majority content of silica, a thermosetting adhesive layer, and a minority portion of PTFE. Figure 11 shows the test vehicle used to characterize a non reinforced silica dominated prepreg (FR-27, DF = 0.0017 at 40 GHz) and a fiberglass reinforced ceramic filled PTFE core (≈ 9 wt% fiberglass). Figure 11 is noteworthy because the center core of Nelco4000-13SI stands out from the top and bottom high speed layers having almost no fiberglass reinforcement. Figure 12 shows the digital eye patterns at 12 gbps of the non reinforced prepreg with the ceramic filled Teflon® core versus a reference material comprising rubber, silica, brominated flame retardant, and ≈ 33 wt% fiberglass, known in the industry as hydrocarbon. The rubber based substrate shows an eye height of 244 mV versus 369 mV for the Teflon® containing substrates. The rise time is more noteworthy. The PWB based on the non-reinforced prepreg had a rise time of 43.85 ps vs 65.95 ps for the rubber based PWB. This large difference in eye height and rise time is more pronounced at 12 gbps than was published in another investigation published elsewhere[3], where the gains in the 10 gbps range weren't as obvious. Each of these eye patterns is taken with a PRBS 2^31 pattern along a differential 4.25 inch trace at 12 GB/s. The rubber based substrate had an insertion loss of -5.5 dB while the PWB containing the non reinforced substrate had an insertion loss of -2.3dB. Identical trace lengths of 14 mil width were used.

1. Lee Richie, "Impact of Glass Weave on Skew and Jitter", copyright Speeding Edge, February 13th, 2007

2. Jeff Loyer; Richard Kunze, and Xiaoning Ye, "Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies", IEC DesignCon 2007

3. Heidi Barnes, Jose Moreira, Thomas McCarthy, William Burns, Cresencio Gutierrez, Mike Resso, "ATE Interconnect Performance to 43 Gbps using Advanced PCB Materials", IEC DesignCon 2008.

Figure 1. *fast*Rise27 prepreg between two FR-4 cores

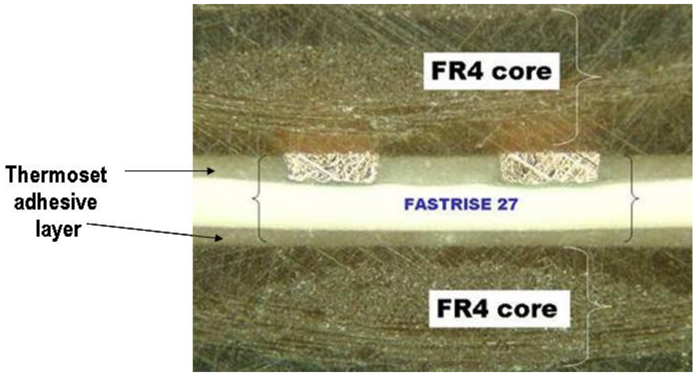


Figure 2. 20 layer PTFE based PCB reinforced with 106 fiberglass.

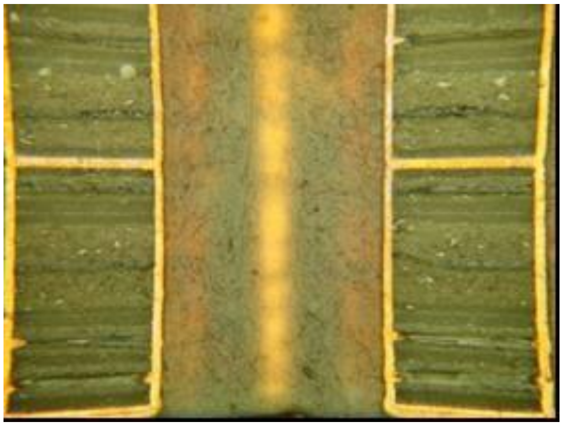


Figure 3. Photomicrograph showing what looks to be PTFE hairs or fibers attached to an interconnect pad protruding out into a sidewall.

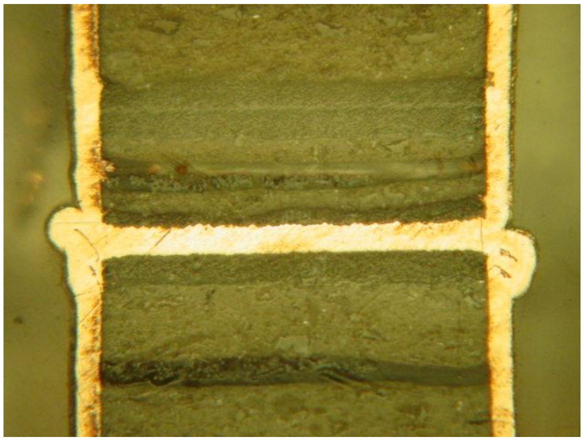


Figure 4. A scanning electron micrograph and EDX scan of a defect in an 18 layer PCB where the electron beam is focused into the void.

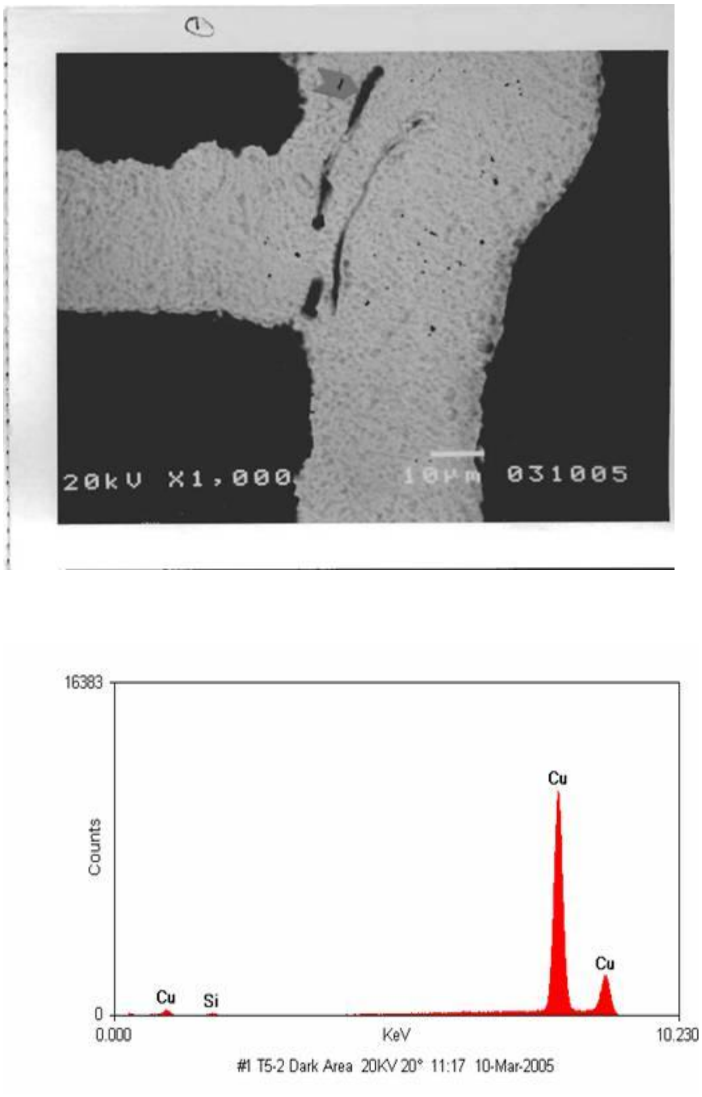


Figure 5. Scanning electron micrograph and EDX scan of an 18 layer PCB after the board has been sectioned and the copper plating removed by etching leaving the bare hole wall and potting compound in place.

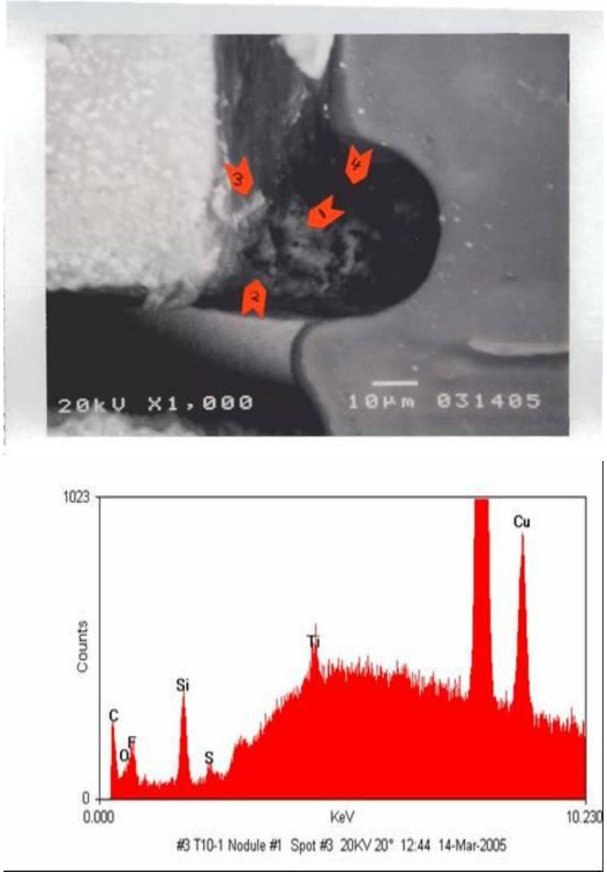


Figure 6. Scanning electron micrograph of sidewalls after the interconnect pad and the plated copper have been etched away showing perhaps drill bit debris that has been compacted into the sidewalls.

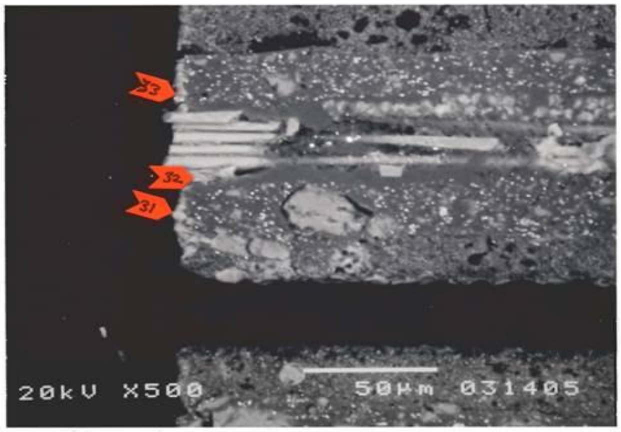


Figure 7. Optical micrographs of a 20 layer PWB with drilled holes before plating.

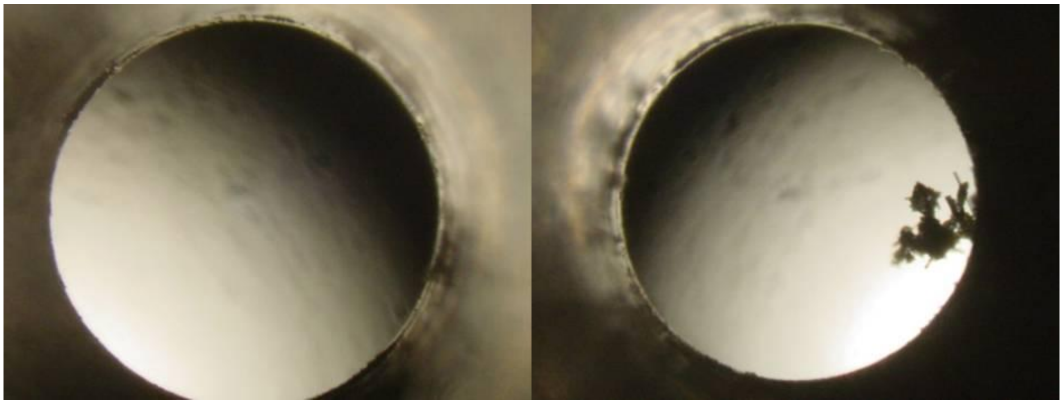


Figure 8 Twenty mil diameter straight shank drill bit completely inundated with drill bit debris

Figure 9a 20 hits into PWB (left), 20 hits into phenolic (right)

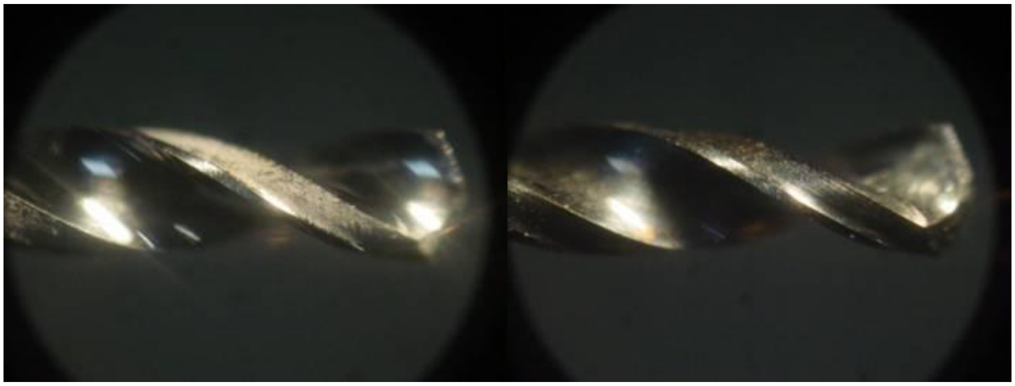


Figure 9b 100 hits into PWB (left), 100 hits into phenolic (right)

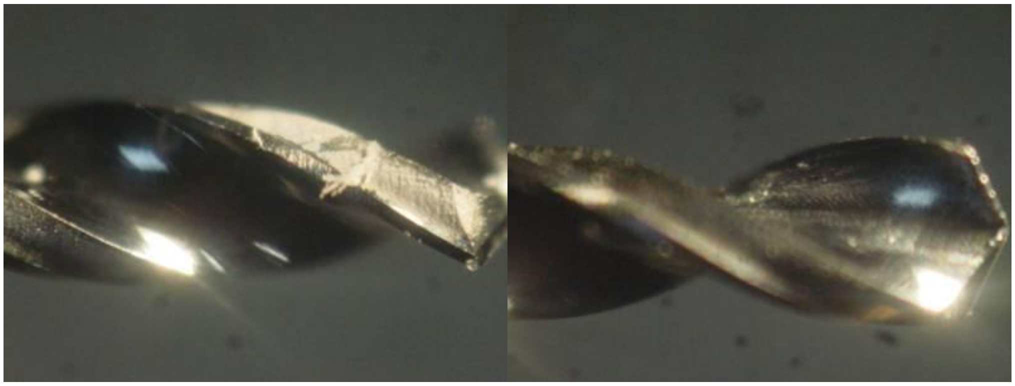


Figure 10 Example of good (left) and bad (right) 10 mil drill plated through holes

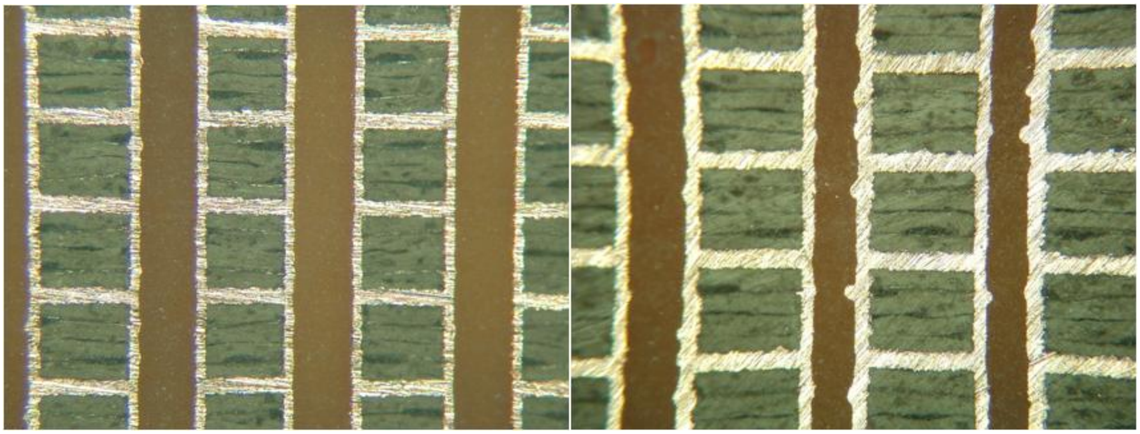


Figure 11. Photographs of the entry (left) and exit (right) sides of a drilled circuit board with 10 mil holes. Notice the holes on the exit side are displaced as a result of drill wander.

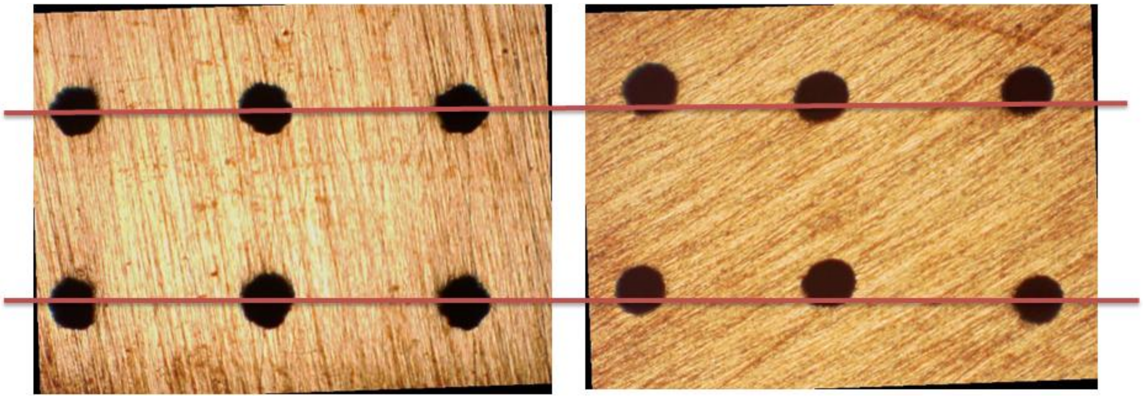


Figure 12. Poor registration around a pad caused by drill wander.

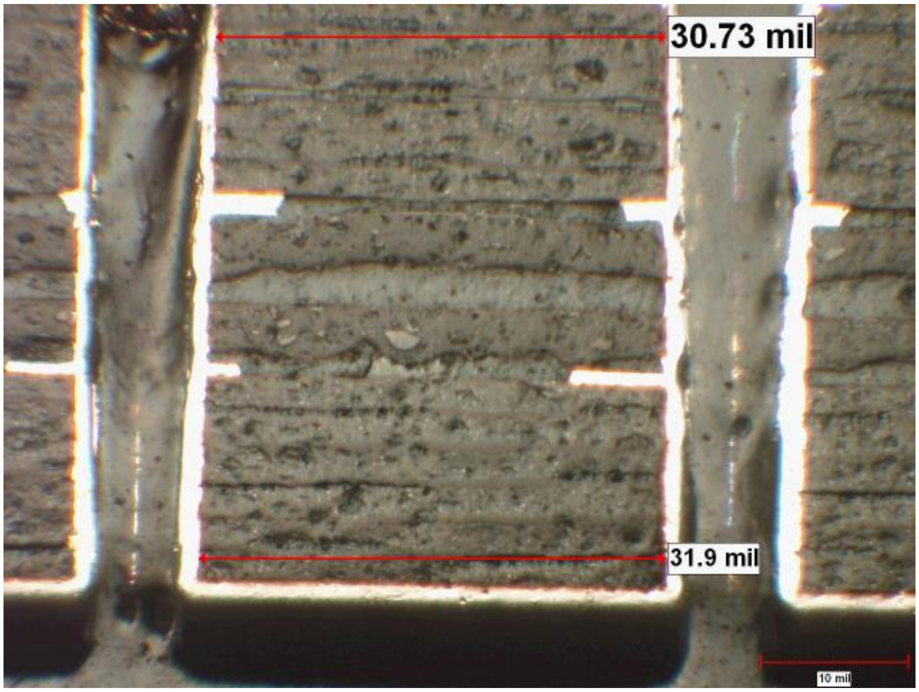


Figure 13 Hybrid test vehicle containing a non-reinforced fiberglass free prepreg (FR -27), a glass reinforced ceramic filled Teflon® core (TSM-29), and a center core of Nelco 4000-13SI easily denoted by the heavy fiberglass weave.

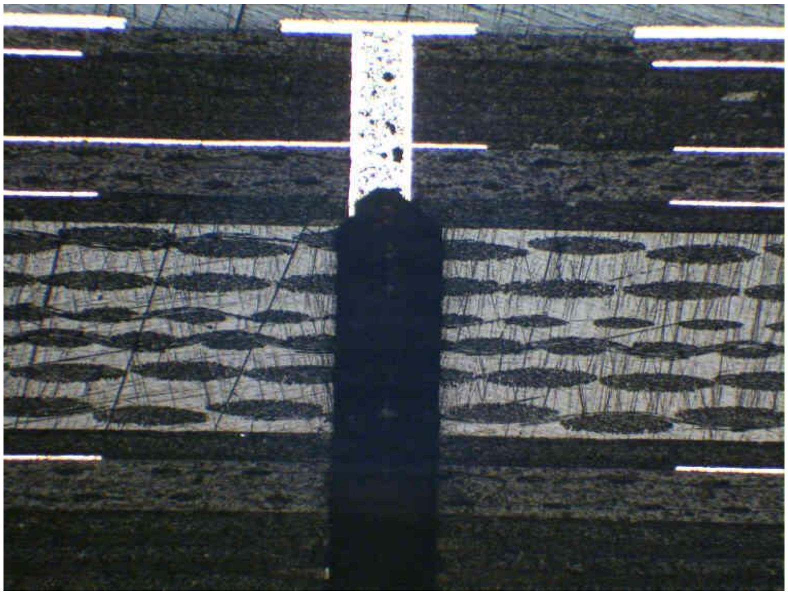
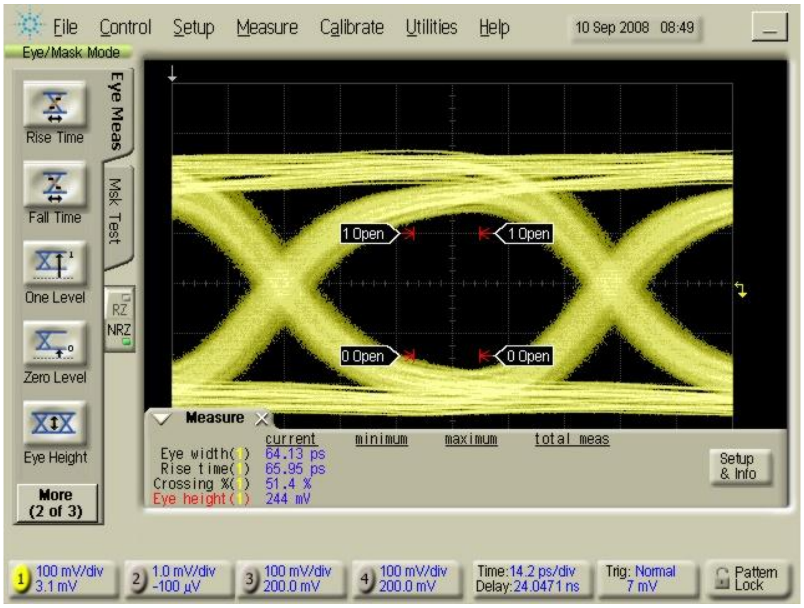


Figure 14 Digital Eye patterns at 12 gbps of a fiberglass reinforced laminate comprising rubber, a brominated flame retardant, and silica (top, known in the industry as hydrocarbon) versus the same test vehicle manufactured from a fiberglass reinforced ceramic filled Teflon® core and a non-reinforced silica dominated low temperature prepreg (bottom).



```
            current    minimum    maximum    total meas
 Eye width( )  64.13 ps
 Rise time( )  65.95 ps
Crossing %( )  51.4 %
Eye height( )  244 mV
```

```
1 100 mV/div 3.1 mV   2 1.0 mV/div -100 µV   3 100 mV/div 200.0 mV   4 100 mV/div 200.0 mV   Time:14.2 ps/div Delay:24.0471 ns   Trig: Normal 7 mV
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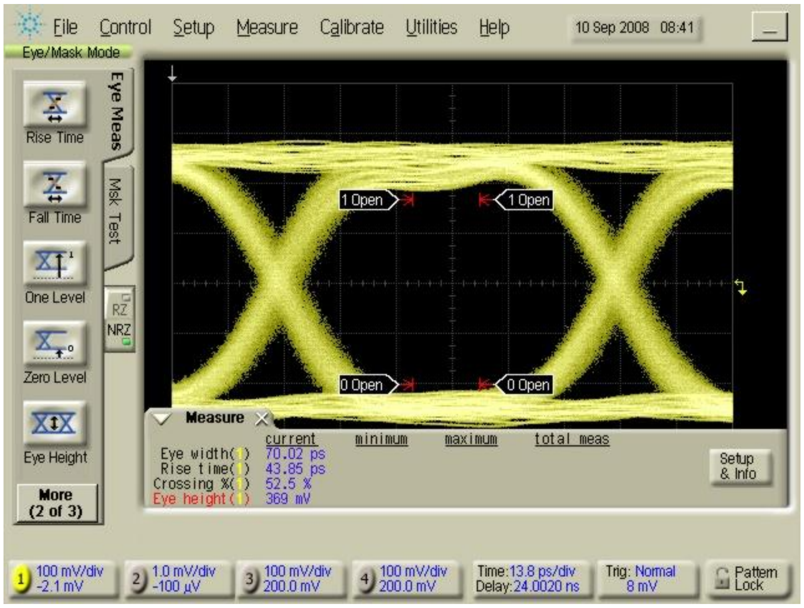

```
            current    minimum    maximum    total meas
 Eye width( )  70.02 ps
 Rise time( )  43.85 ps
Crossing %( )  52.5 %
Eye height( )  369 mV
```

```
1 100 mV/div -2.1 mV   2 1.0 mV/div -100 µV   3 100 mV/div 200.0 mV   4 100 mV/div 200.0 mV   Time:13.8 ps/div Delay:24.0020 ns   Trig: Normal 8 mV
```