DesignCon 2003

High-Performance Systems Design Conference

Signal-Integrity Measurements Support the Candidacy of PTFE at High Data Rates

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Abstract
A growing need is developing in the high speed digital arena (backpanels, motherboard, line cards etc) for high performance laminate, prepreg materials, connectors, intelligent routing of differential pairs, and other strategies to improve signal integrity at the 10 gbps range. Polytetrafluoroethylene (PTFE) has a long history of meeting the needs in radio frequency applications up to 77 GHz. PTFE based materials reinforced with woven glass fabric have traditionally offered the advantage of very low loss (<0.003 @ 10 GHz). The laminate and prepreg material that will be used as a baseline for signal integrity measurements (SI) is a PTFE/fiberglass/BT-epoxy composite (TacPreg™)[1] that offers a dissipation factor from 0.004 to 0.005, depending on BT-epoxy resin content, at 14.5 GHz. Described in this paper are SI measurements carried out using standard practices that rely on eye openings and jitter using a 20 layer 170 mil thick backplane test vehicle. The signal integrity of the test vehicle is dependent on the total system, the FR4 daughtercards, the SMA connectors, and Teradyne's GBX™ connectors[2]. The future of design is taking some tips from microwave engineers where insertion loss, (loss in signal in dB/inch) is routinely characterized. The PTFE/fiberglass/BT-epoxy laminate was evaluated in a separate test vehicle with no daughter cards to best characterize the laminate under test. The loss in power (dB) for different trace lengths was then investigated at different frequencies. All the data suggests that the combination of a high performance laminate in a properly designed system with the optimal connectors will offer superior performance at 10 gbps and higher. Preliminary data suggests that the laminate material will cost 4.0x FR4 and finished printed circuit boards will cost OEM's 1.6-1.9x FR4, depending on volume. Preliminary processing information further suggests that although there are a few steps such as plasma treatment of drilled holes before electrolysis, the PTFE/fiberglass/BT-epoxy processes similar to BT-epoxy with a few changes in fabrication that must be made for the high PTFE content.

Authors Biographies
Thomas McCarthy received his bachelor's degree in Chemistry from Wesleyan University in 1988, his PHD in polymer science and engineering from the University of Massachusetts, Amherst, in 1993, and an MBA from Rensselaer Polytechnic in 2001. Tom worked for one year as a visiting scientist at the Max Planck Institut for Polymer Research, Mainz Germany, from 1993-1994. Tom spent nearly 6 years at the AlliedSignal Corporation located in Morristown, NJ. Tom has numerous patents and publications in the area of fluoropolymers and electronic materials. Tom is currently the Product Manager for TacPreg™ and the Technical Manager for Taconic's US Operations.

Meagan Morrell is currently a Signal Integrity Engineer in the New Products Development Group at Teradyne, Inc. Meagan currently integrates products from silicon and laminate vendors with Teradyne's interconnect products. Her other functions include customer applications support and backplane interconnect testing. Ms. Morrell has a BS in Electrical and Computer Engineering from the University of New Hampshire.

Joe Tripi received his bachelors in industrial engineering from Northeastern University in 1973 and since then has a long work history (20+ years) in the printed circuit board industry including: Digital Equipment Corporation from 1977-1983, Alto-tronics from 1989-1991, San Mina from 1994-2000, and most recently Teradyne Connection Systems. Between those experiences Joe has also worked as a consultant and owned an equity position in a small printed circuit board shop called CTCN as a partner. Most recently Joe has been responsible for new materials investigation for Teradyne Connection Systems.

Introduction

The marketplace for laminates has in the past generally distinguished microwave or RF type applications from digital applications. RF applications involve analog signals operating at very high frequency, with 77 GHz for collision avoidance systems being not that unusual. Digital signals have conventionally relied on FR4 like materials operating up to 2.5 Gbps. The fun starts when designers look to design digital systems at 10 Gbps and beyond. RF engineers have traditionally turned to polytetrafluoroethylene (PTFE) based laminates for the highest level of performance. Applications such as low noise block converters or cellular phone base station antennae need ultra low loss materials to handle the weak signals that must be filtered and amplified. The printed wiring boards that dominate the RF world are double sided or less than 6 layer boards, have large trace geometries, and are not densely packed. For these reasons, RF engineers can turn to more expensive materials. Digital designers, on the other hand, turn to printed wiring boards having significantly higher layer count, small plated through holes, and higher density. Therefore, the digital designer has a preference for (a) low cost materials and (b) due to the complexity of the printed circuit boards, robust materials such as epoxy. However, as OEMs target 6.25 and 10.0 Gbps data transmission rates, the usual bin of materials doesn't appear to have the legs to keep working indefinitely without compensating with some technology that has its own set of advantages and disadvantages. Digital designers have to start considering the tradeoffs between migration to higher performing laminates and better devices. There will always be the desire to design FR-4 forever. However, at some point the cost required to enable FR4 to operate at frequencies of 10 Gbps and higher will exceed the cost of changing laminate materials.

It is no big surprise that PTFE can satisfy the future electrical requirements of the high speed digital space. The questions that need to be addressed are…. can a PTFE-based solution be offered that can be fabricated world-wide, be robust enough in leading edge designs (12:1 aspect ratio plated through holes on thick boards), at a price that is attractive enough to compete with alternative technologies? This article will describe the following: (1) trends in future design that support the use of PTFE for future digital designs (2) a PTFE/fiberglass/adhesive based laminate that satisfies those future requirements (3) fabrication considerations of the PTFE/fiberglass/adhesive into a 20 layer backpanel (4) laminate properties of the PTFE/fiberglass/adhesive (5) reliability testing of the 20 layer backpanel (6) Does the thermal expansion of PTFE pose a reliability problem? (7) for comparative purposes, signal integrity measurements of FR4 with and without a passive equalizer at high data rates (8) signal integrity measurements of a PTFE/fiberglass/adhesive based backpanel with FR4-daughtercards up to 10 Gbps, with and without equalization (9) the dependence of loss (db) on frequency and trace length for signals launched onto a printed wiring board up to 30" in length and (10) eye patterns of a test vehicle using no daughter cards, where the signal launched directly onto board (11) and the cost multiple of a printed wiring board made with the PTFE/fiberglass/adhesive vs FR4. A case will be made that FR4 may not be the preferred choice at higher speeds and longer lengths over PTFE based composites.

Design Trends

Material suppliers are being challenged by engineers to offer the following characteristics for high speed data transmission applications (1) increasingly lower loss (2) thinner and thinner dielectrics and (3) low cost. Signal loss occurs due to the resistive loss of the copper trace, the skin effect, and the losses associated with the material itself, polarization of the molecules making up the dielectric material. Dielectic loss is captured in the concept of the loss tangent. The loss associated with the dielectric material dominates these losses in the GHz range[1,2]. The loss contributed by the dielectric material is proportional to the products of the frequency, the loss tangent, and the square root of the dielectric constant.

$$\alpha_d = \pi * \tan\delta / \lambda_g$$

$$\alpha_d = K*f* \tan\delta \text{ *square root of } \varepsilon_r$$

where α_d = the dielectric loss, λ_g = the wavelength along the conductor, K = a constant, and ε_r = the dielectric constant[3]

Therefore, high data rate transmission will favor materials with increasingly lower loss and lower dielectric constant. Dielectrics with lower dielectric constants also offer a more practical benefit. Low dielectric constant materials enable the transition to thinner dielectrics. Backpanels and daughter cards are in demand at increasingly higher layer count leading to thicker and thicker pwbs. Cutting edge designs employing the shielding of edge-coupled traces, a pseudo coax cable shielded differential pair, only add to the complexity of the boards. Designers recognize that the plated through hole itself is a source of parasitic capacitive losses and work is being conducted to shift to controlled depth drilling, buried and blind vias. Lower dielectric constant materials should enable a shift to more complex designs using a larger number of thinner dielectrics. PTFE should be well suited to accommodate these demands.

The one design trend that clouds the future is the use of active and passive devices to enhance signal quality. The use of these devices is challenged by the possible amplification of reflections and standing waves, cost, board space, and the handling of increased power levels. One such device, a passive receive side equalizer, is demonstrated in this report. These passive receive side equalizers act as low pass filters where some loss in amplitude is to be expected. The race to supply a device has far more silicon competitors than there are laminate material suppliers. However, there is the potential for the use of active/passive devices in combination with high performing laminates when transmitting data at very high data rates.

PTFE/fiberglass/adhesive-based Prepreg and Laminate

The cost of traditional PTFE/fiberglass composites has dropped dramatically in recent years due to the maturing telecom infrastructure (base station power amplifiers, antennae etc). The patent pending PTFE/fiberglass/adhesive

technology overcomes the last hurdle that the demand from the large telecom OEMs did not. The PTFE/fiberglass/adhesive approach overcomes the volume manufacture of PTFE laminates. The composite consists of PTFE, a fiberglass reinforcement, and an adhesive. The composite is shown in Figure 1.

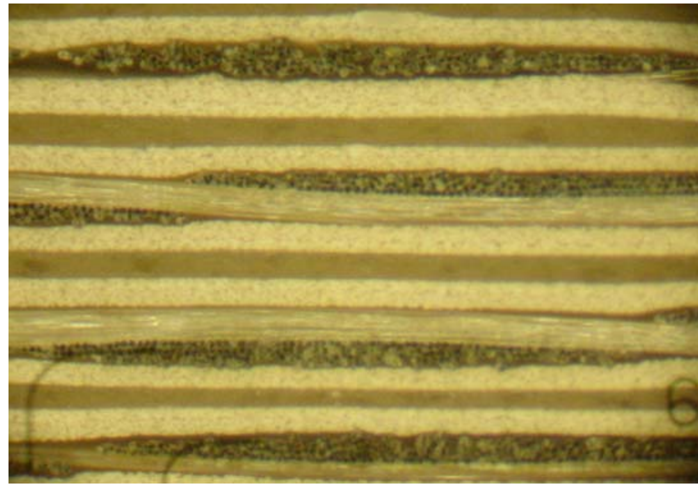

Figure 1. Cross Section of the PTFE/fiberglass/adhesive

PTFE has generally been considered an expensive material because of the following factors (1) the nine hour press cycles to produce a PTFE based laminate vs 3 hours for an FR4 laminate, (2) the lack of infrastructure to prepare laminates on massive scales consistent with FR4 lamination (3) the job shop like mentality that existed to service small military and RF applications. This is overcome by drawing on the resources of one of the worlds largest FR4 processors (Isola AG) to apply the adhesive and convert it into laminate. Using this model, fiberglass is impregnated with PTFE by a high volume PTFE composites manufacturer, after which the substrate is treated with an adhesive layer and laminated worldwide. The adhesive layer is a thin coating of a thermosetting resin used to obtain layer-to-layer adhesion. The adhesive layer only needs to be thick enough to fill the gaps in the copper circuitry and provide a robust interconnect amongst the otherwise PTFE dominated layers. The adhesive can be any robust material currently used in printed wiring boards. These could include any of the following, for example: FR4, BT-epoxy, cyanate ester, etc. The PTFE/fiberglass/adhesive presently is formulated with a BT-epoxy that is known to be a very reliable resin system employed in semiconductor packaging systems. BT-epoxy is known for its good peel strengths, improved electrical performance over FR4, and low coefficient of thermal expansion. Basically, the PTFE/fiberglass/adhesive combines the robustness of PTFE with the process attributes of an equally robust BT-epoxy. From a fabrication perspective, the fabricator can use standard methods of epoxy processing with some allowances made for the high PTFE loading. The printed wiring board is laminated at FR4 like temperatures and pressures. Traditional innerlayer treatments can be used because the surface of the board is BT-epoxy. Copper foil is bonded to the BT-epoxy adhesive and not the PTFE. However, because of the high loading of PTFE, fabricators must use modified drilling parameters and hole wall treatment, all within the competencies of today's fabricators. OEMs have expressed some concerns about the supply chain and dual sourcing. Supply chain is of particular concern for a lot of exotic materials because they are single sourced. Dual sourcing is accomplished by combining the worldwide infrastructure of a PTFE coater with the worldwide infrastructure of multiple FR4 laminators.

Fabrication

The lamination cycle for the PTFE/fiberglass/adhesive is shown in Figure 2.

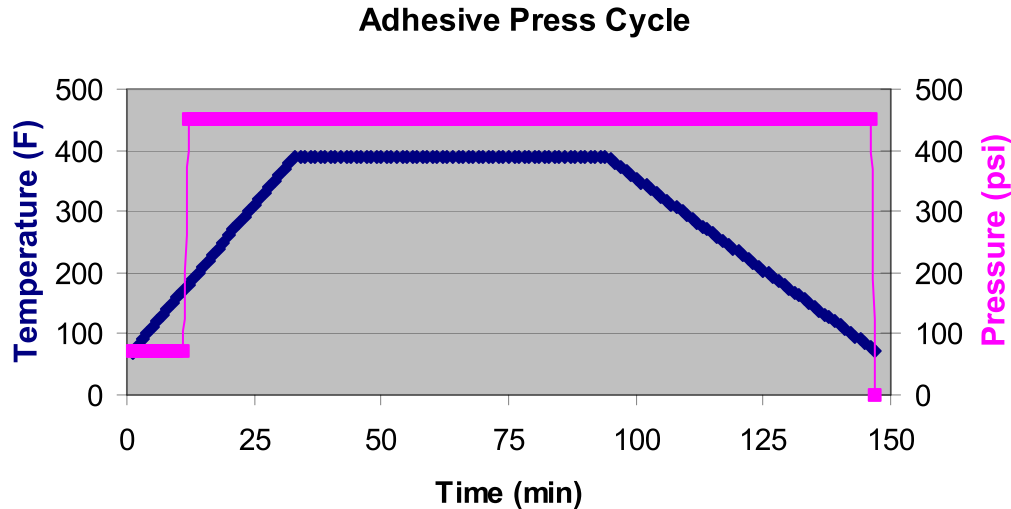

Figure 2. Lamination Cycle for PTFE/fiberglass/adhesive

It should be acknowledged that PTFE based laminates do not fabricate like FR4. PTFE must be treated with plasma before metallization. However, because most major fabricators have plasma capability this is not a limitation. PTFE is also more difficult to desmear. PTFE must be drilled well to eliminate the need for extensive plasma desmear. PTFE should be drilled with new drill bits to maintain a sharp cutting surface. Some fabrication information has been published[4]. It is fair to say that recommendations exist for all board level processing of PTFE. While there are some minor nuances, there are no more challenges than for fabricating other higher performing materials. For example, PTFE based hybrids do not share the following challenges that some of its competitors suffer from: (1) poor hit counts during drilling, the number one cost to a fabricator, (2) reduced copper adhesion that is a serious problem for rework, (3) limited soldermask adhesion requiring surface preparation, less than desirable reliability after thermal cycling due to a further degradation of copper bond strength and (4) smeared PTFE fiber left in hole walls (non-woven PTFE fiber). Designers increasingly prefer lower profile copper foils that will particularly challenge some laminate suppliers that already suffer from low copper peel strengths.

Laminate Properties of the PTFE/fiberglass/adhesive

Laminate properties of the composite are shown in Appendix A, Table 1. The dielectric constant is approximately 3.2 and is relatively flat over frequency (Figure 3).

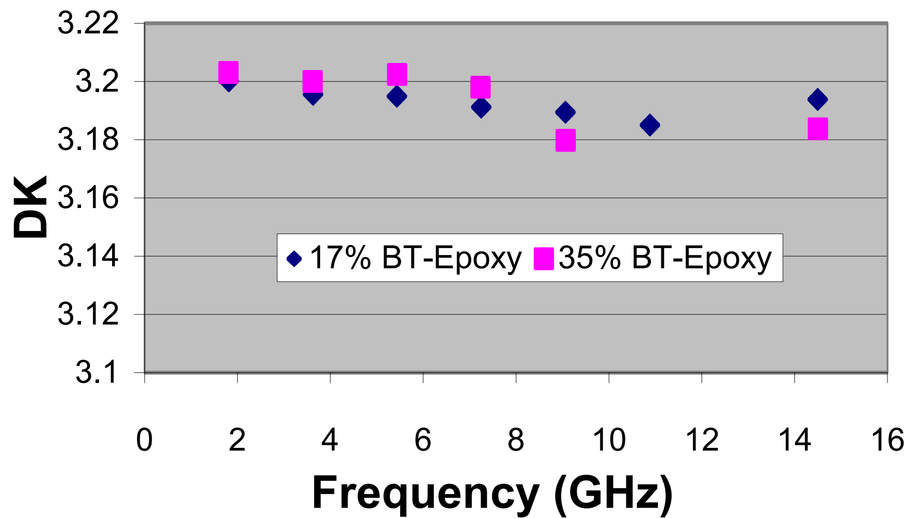

Figure 3. Dielectric Constant of the PTFE/fiberglass/adhesive over Frequency

The loss tangent varies from 0.004 to 0.005 depending on the amount of adhesive used (Figure 4) and is also very flat over frequency.

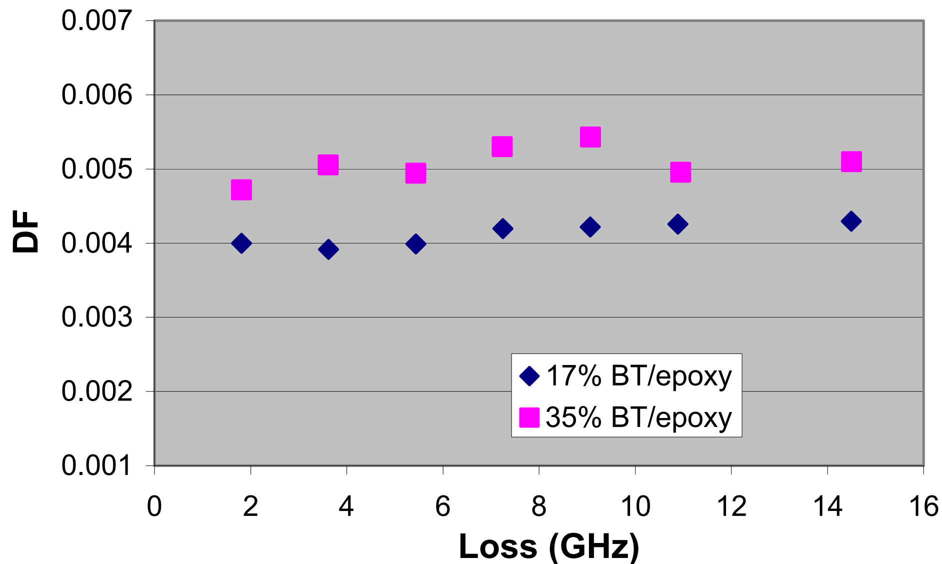

Figure 4. Loss Tangent of the PTFE/fiberglass/adhesive over Frequency

Very low loadings of adhesive (15 wt%) can be used to fill the gaps in 0.5 oz circuitry, while higher levels are needed for 1 and 2 oz. copper respectively (25 and 35 wt% epoxy). Because the composite has a weight percent ratio of roughly 5:1 of PTFE to epoxy, after subtraction of fiberglass and various fillers, one can measure a very weak glass transition of the epoxy. However, one should expect

the room temperature relaxation of the PTFE to dominate the temperature dependent mechanical properties.

Reliability Testing

Reliability testing to date has focused on 6x solder floats, time to delamination tests at 260°C, 288°C, and 300°C, and the liquid-to-liquid thermal shock tests. To date there have been no 6x solder float failures on 20 layer backpanels built for demonstrator purposes. The T260, T288, and T300 test measurements are shown in Appendix A, Table 1. All of the time to delaminations exceed the time of testing. The liquid-to liquid thermal shock test IPC-TM-650, method 2.1.1D, was conducted by Trace Laboratories-East. Specimens were placed in a liquid-to-liquid shock test chamber. The test conditions were as follows: low extreme of –35°C, high temperature of 125°C, 10 minute dwell at each temperature, 15 second transfer time between temperatures, 400 cumulative cycles. After completion of 100, 200, 300, and 400 cycles, representative specimens were removed from the test chamber. The specimens were then prepared for microsection analysis. Two different lots of backpanels were tested. A representative photo after a 400 cycle exposure is shown in Figure 5. While it must be acknowledged that the bare-boards contained some drilling related challenges, the report from Trace laboratories can be summed up by the following points: (1) There were no plating cracks observed on any of the samples after 100, 200, 300, or 400 cycles (2) no evidence could be found for thermally induced pad lifting (3) Defects found in the sections were related to bare board fabrication and were not thermally induced. These results suggest that while there are some fabrication challenges to be optimized, backpanel interconnects are robust over a 400 cycle liquid-to-liquid thermal shock test. Parts are currently being built for interconnect stress testing (IST).

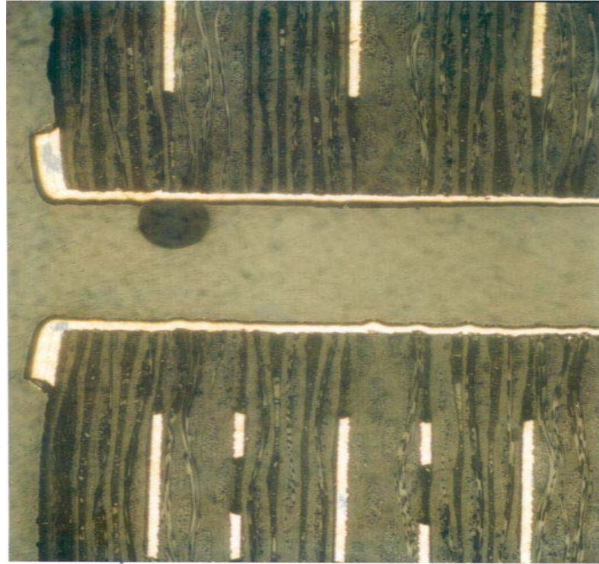

Figure 5. Photograph of PTFE/fiberglass/adhesive composite after liquid-to-liquid Thermal Shock, Lot Number TR2-00-050158-01-01 at 400 cycles, showing no lifted lands or plating cracks at 50X.

Is the Thermal Expansion of PTFE a Reliability Problem?

PTFE has a higher coefficient of thermal expansion than many thermosetting resins. PTFE based laminates can have a z axis CTE from 70 to 300 ppm/°C. Engineers are tuned to the relationship between CTE and reliability for thermosetting resins and believe that a higher z axis CTE means less reliability. For thermosetting resins that can be described as incompressible fluids, correlations can be made between z axis CTE and the number of thermal cycles a plated through hole will survive (IST testing). PTFE does not have a glass

transition somewhere between 100 and 200°C and therefore the CTE does not jump from 70 ppm/°C to 300 ppm/°C as does FR4 as it nears its Tg. For thermal excursions of 260-280°C, PTFE has a lower Z axis expansion when calculated over the entire range, even though the epoxy has a lower Z axis CTE below its glass transition.

But what does all this mean? PTFE is a collection of discrete fused particles that make physical contact with each other at points but otherwise PTFE is filled with air due to the particle to particle voiding (Figure 6). PTFE is a soft polymer that is a compressible material. During the sintering of PTFE, it does not melt and flow, the PTFE particles only compress.

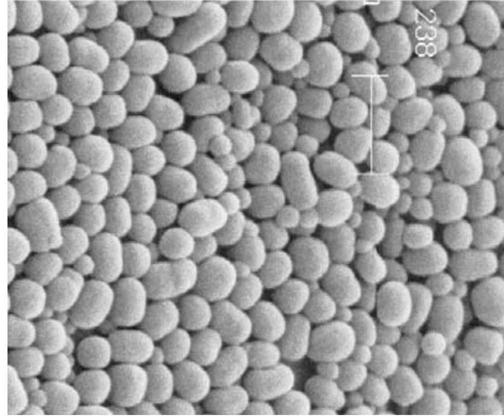

Figure 6. Scanning electron photomicrograph of PTFE particles

Engineers are interested in the thermal reliability in the range of sub zero temperatures to around 125°C (liquid-to-liquid thermal shock). When the temperature is increased from room temperature one would expect PTFE to expand. An increase in temperature should lead to an increase in expansion (strain) that should lead to a linear increase in stress on a plated through hole. But wait, the modulus of PTFE is hardly constant as the temperature increases. The tensile modulus of PTFE from room temperature to 100°C decreases by two orders of magnitude from 340 GPa at room temperature to 0.69 GPa at 100°C. Therefore, as the temperature increases and the PTFE expands, the decreasing modulus will lead to less stress on a plated through hole and the unexpected reliability in the liquid-to-liquid thermal shock test. Thermosetting resins such as epoxies are very different[6-8]. The tensile modulus of a crosslinked polymer falls modestly or not at all for a high Tg resin over the temperature range from RT to 100°C. Therefore, because the modulus drops far less for an epoxy based thermoset than for PTFE and the epoxy is amorphous and can be described more like an incompressible fluid, the resulting expansion of an epoxy would be expected to exert more stress on a plated through hole.

Signal Integrity Measurements at High Frequencies

A 20-layer test vehicle designed especially for SI measurements was prepared by Teradyne Connection Systems. The 20-layer test vehicle can be seen in Appendix B, Figure 1. The 20-layer test vehicle consists of alternating signal and ground planes (foil lamination). The SI vehicle is designed as follows: 18 x 24", 1 oz copper, 8 mil innerlayer cores of a PTFE/fiberglass composite or a PTFE/fiberglass/adhesive composite, bonded together by 3 plies of the PTFE/fiberglass/adhesive prepreg, trace geometry includes 8 mil widths with 8 mil spaces, an impedance of 100 ohms, using an edge coupled differential stripline configuration (the traces having a ground plane above and below to yield the stripline configuration), and copper traces of 10 and 20 inches in length. The

layers were pressed together using processing conditions similar to those recommended in Figure 2. The hole walls were treated with plasma for the PTFE based boards.

SI measurements were made by attaching two FR4 daughter cards to the backpanel using Teradyne's GBX™ connectors. The random sequence of bits are generated by a HP70340A Signal Generator (HP70004A display, 1-20 GHz) connected to a daughter card by cable and SMA connector. The signal then exits the daughter card through a GBX™ connector into the backpanel under test. After conduction along a 10" or 20" copper trace, the signal exits via a GBX™ connector to another daughter card. The full signal is then routed back to an Agilent Oscilloscope (Agilent 86100A Wide-Bandwidth O-scope) where the signal is sampled differentially and displayed in real time. All measurements were taken with a 500 mV voltage swing with a 250 mV peak and a 2^{23}-1 PRBS pattern. It should be understood that the signal integrity tests are a function of the entire system, not just the backpanel. The 5 layer FR4 daughter cards, for example, will impart appreciable loss to the system. Recognizing that there is a system loss independent of the laminate under test, the configuration is good for comparing different laminate materials used to make the backpanels. For tests including the Gennum GN2001 equalizer, the signal exits the backpanel via a GbX connector to a second daughter card integrating Gennum's GN2001 10 Gbps equalizer chip between the GbX connector and SMA connector. (This daughter card requires a voltage source, Agilent E3632A, using 3.3 volts and a current limit of 50 mA per chip.)

TDR measurements were made by setting the Agilent 86100A Wide-Bandwidth O-scope to the TDR mode, calibrating, and then normalizing for differential TDR measurements. The differential pair of cables from the Agilent sends a signal into the desired pair on daughter card A, the signal is launched along the pwb, is then routed through daughter card B that is terminated with a 50 ohm load. The reflected data is then measured on daughter card A. (This shows the impedance of all inconsistencies within the system tested, please see Appendix B, Figure 2.)

At what frequency does FR4 reach its natural limitations?

The combination of 2 FR4 based daughter cards, 3 inch trace lengths per daughter card, has a very small eye at 7.5 Gbps using a 10" FR4 based backpanel (Figure 7). The signal is improved considerably when a Gennum GN2001 device is used on the receive side of the backpanel (Figure 7), showing at least 300 mv of eye opening. Because the GN2001 is a passive device that separates out some of the high frequency signal, some loss in amplitude is expected.

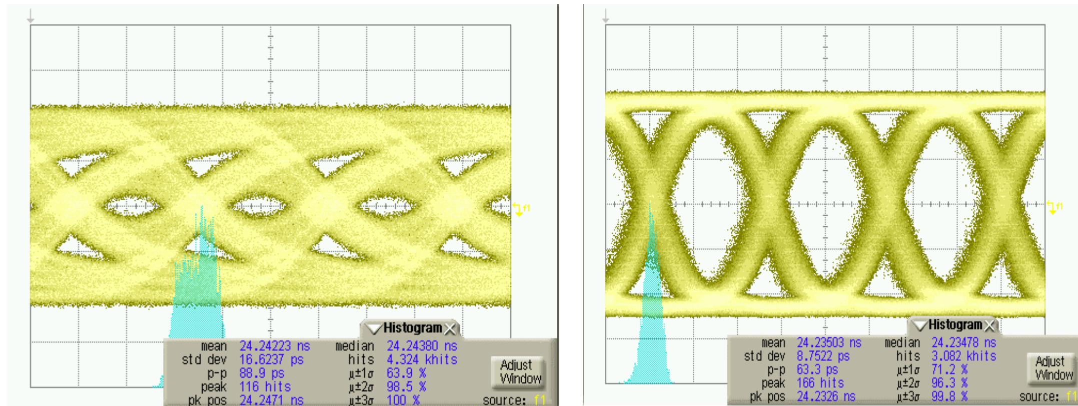

Figure 7. Backpanel using 10" traces on FR4, DE12, FR4 daughter cards, at 7.5 Gbps (left) with a 200 mV/div vertical scale, and using a Gennum 2001 (right) equalizer with a 100 mV/div vertical scale. SI measurements taken differentially.

The same FR4 based 10" backpanel operating at 10 Gbps has virtually a closed eye at 10 Gbps (Figure 8). The Gennum GN2001 manages to salvage a signal having an open eye of about 200 mv with a jitter of 67 ps at 10 Gbps (Figure 8). Again, a 10" trace is a very short trace for a backpanel.

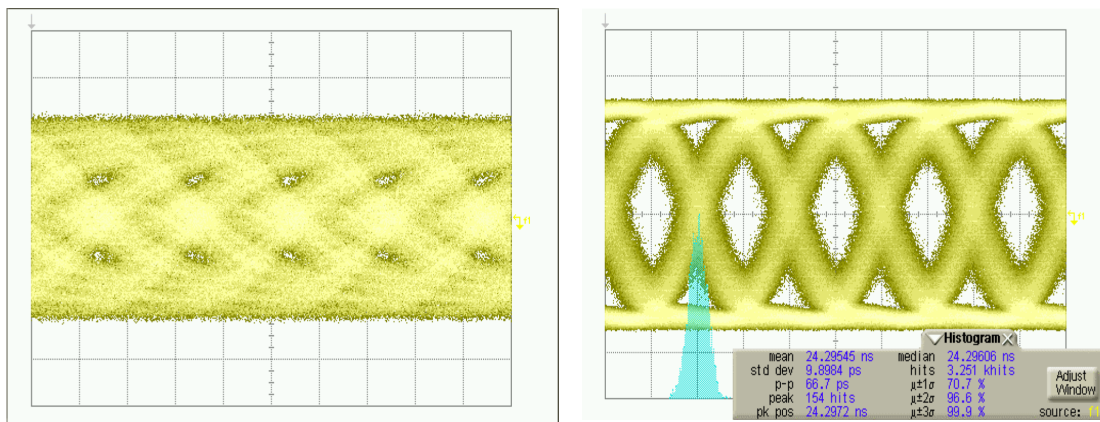

Figure 8. Backpanel using 10" traces on FR4, DE12, FR4 daughter cards, at 10.0 Gbps (left) with a 200 mV/div vertical scale, and using a Gennum 2001 (right) equalizer with a 100 mV/div vertical scale. SI measurements taken differentially.

The same configuration using a 20" copper trace on FR4 has completely closed eyes at 7.5 and 10 Gbps (Figures 9 and 10). The same backpanel operating with the assistance of the GN2001 has an open eye of about 200 mV at 7.5 Gbps (jitter = 93 ps) and a virtually closed eye at 10 Gbps.

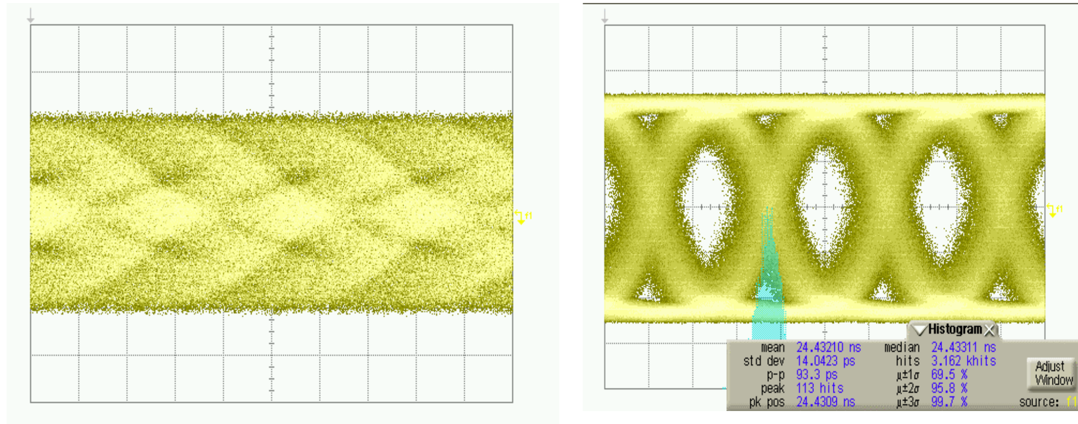

Figure 9. Backpanel using 20" traces on FR4, DE12, FR4 daughter cards, at 7.5 Gbps (left) with a 200 mV/div vertical scale, and using a Gennum 2001 (right) equalizer with a 100 mV/div vertical scale. SI measurements taken differentially.

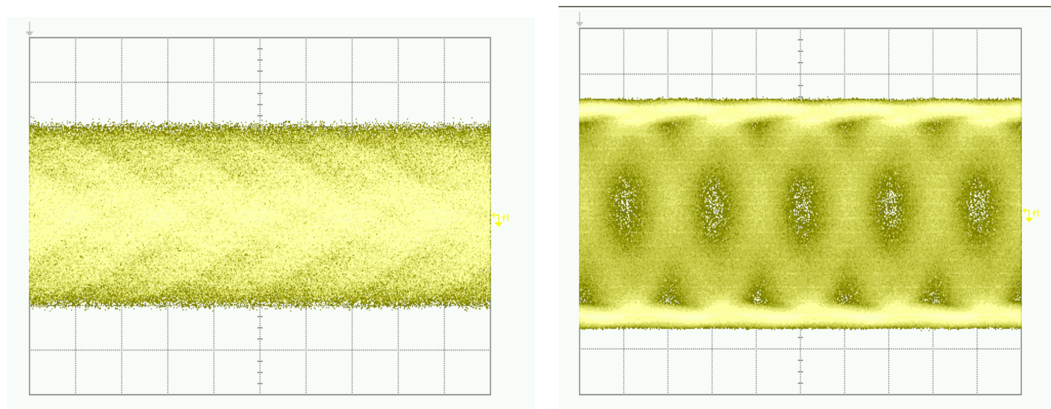

Figure 10. Backpanel using 20" traces on FR4, DE12, FR4 daughter cards, at 10 Gbps (left) with a 200 mV/div vertical scale, and using a Gennum 2001 (right) equalizer with a 100 mV/div vertical scale. SI measurements taken differentially.

Signal integrity measurement of PTFE

Representative eye patterns of the PTFE based materials are shown in Figures 11-14 for backpanels tested from 5 to 10 Gpbs. These eye patterns were all obtained differentially. The backpanels used for signal integrity measurements all used a PTFE/fiberglass/adhesive prepreg as the bonding ply. Signal integrity measurements were taken using PTFE/fiberglass cores* and PTFE/fiberglass/adhesive cores**. Very little difference could be observed using a PTFE/fiberglass composite as an innerlayer laminate core material vs a PTFE/fiberglass/adhesive innerlayer laminate core. As shown in Figures 12-13, there is a significant difference between a 10 and 20" trace at 7.5 Gbps, 216 mV of eye height vs circa 102 mV at 20". At 10 Gbps the eye is virtually closed but

one must consider that the absolute measurements are compromised by the use of FR4 daughter cards and other elements of the system such as the connectors and plated through holes. It is anticipated that if a PTFE based material was used as the daughter cards, better quality jitter and eye height values would be obtained. A later section of this paper shows signal integrity measurements taken launching signals directly onto the backpanel with no daughter cards or connectors.

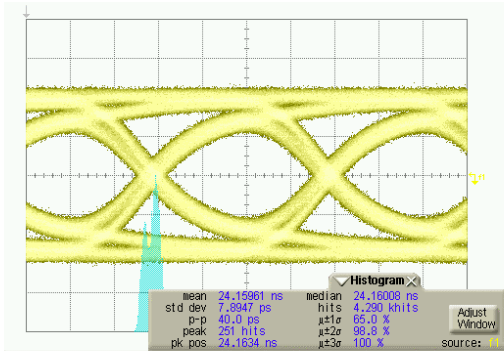

Figure 11. PTFE/fiberglass/adhesive innerlayers bonded together with PTFE/fiberglass/adhesive bonding plies (10 inches @ 5Gbps, 200mV/div) using FR4 daughter cards (444 mV of eye,

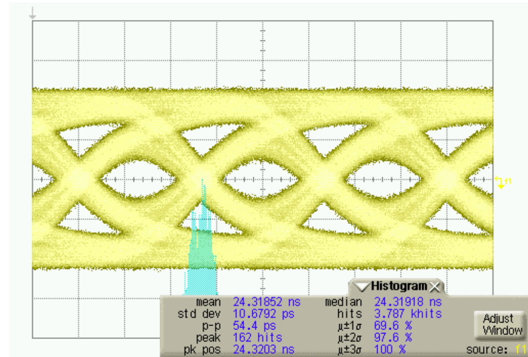

Figure 12. PTFE/fiberglass/adhesive laminates bonded together with PTFE/fiberglass/adhesive prepreg (10 inches @ 7.5 Gbps, 200 mV/div vertical scale) using FR4 Daughter cards (216 mV

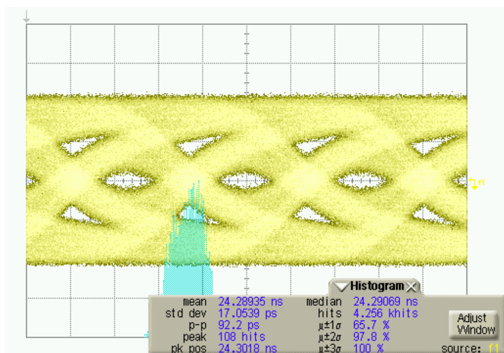

Figure 13. PTFE/fiberglass innerlayers bonded together with PTFE/fiberglass/adhesive prepreg (20 inches at 7.5 Gbps, 200 mV/div vertical scale) using FR4 daughter cards (102 mV

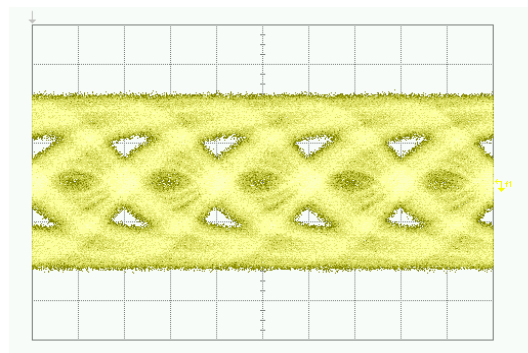

Figure 14. PTFE/fiberglass/adhesive laminate bonded together with PTFE/fiberglass/adhesive prepreg (10 inches@10 Gbps, 200 mV/div,

Figures 15 and 16 show that fairly open eye patterns can be obtained using the PTFE based laminates and prepreg in combination with a passive equalizer even when using FR4 daughter cards. The following section will show that fairly wide open eyes can be obtained at 12 Gbps when the FR4 daughter cards are eliminated and the signal is launched directly onto the backpanel.

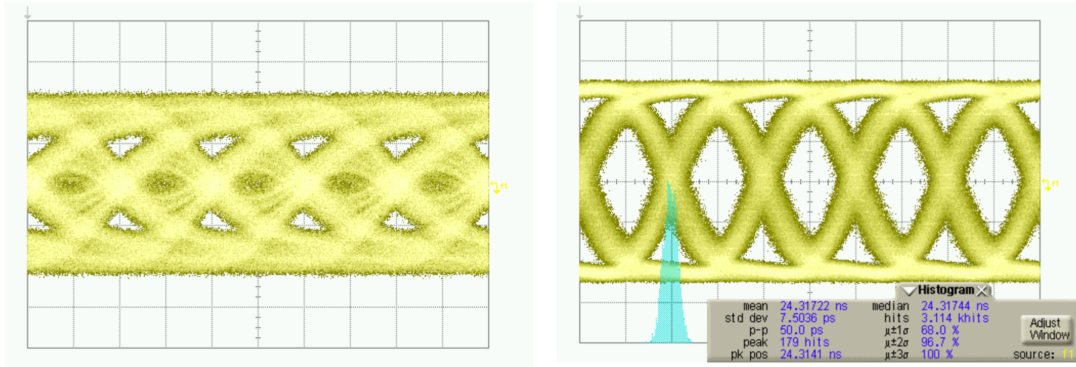

Figure 15. Signal integrity measurements of PTFE based backpanels at 10 Gbps, 10" traces, testing D12/E12 pair (left), and using a Gennum 2001 (right) equalizer (FR4 daughter cards, 200 mV/div for the standard design and 100 mV/div for the system using the Gennum 2001, differential).

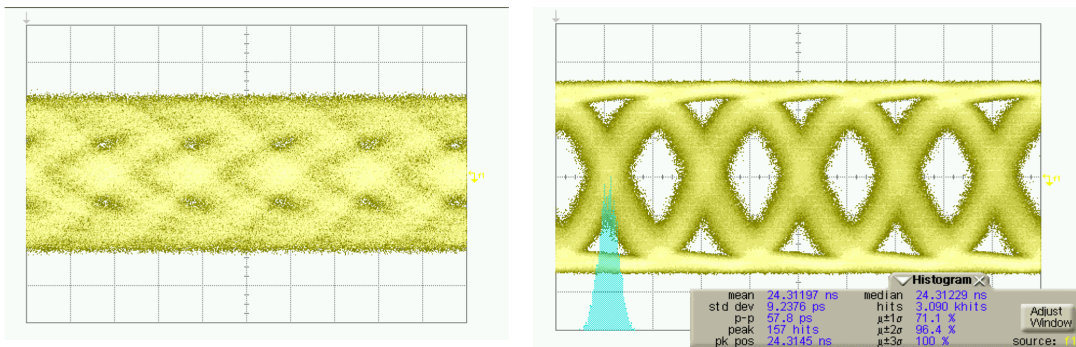

Figure 16. Signal integrity measurements of PTFE based backpanels at 10 gbps, 20" traces, testing D12/E12 pair (left), and using a Gennum 2001 (right) equalizer (FR4 daughter cards, 200 mV/div for the standard design and 100 mV/div for the system using the Gennum 2001, differential).

Loss (db) over Frequency of PTFE/fiberglass/adhesive** vs FR4

Test vehicles were prepared to measure signal loss as a function of trace length (10-30 inches), frequency, and the material under test. These measurements were taken single-endedly. The test vehicles were six layer hybrid builds using a 50 ohm stripline configuration, 1 oz copper. The build used a 10 mil core of the PTFE/fiber/adhesive and 2 bonding plies of PTFE/fiberglass/adhesive in combination with 4 layers of FR4. TDR measurements are shown in Figure 17. This is a much cleaner test. Signals are launched directly onto the backpanel material without losses associated with a poorly performing daughter card. The TDR

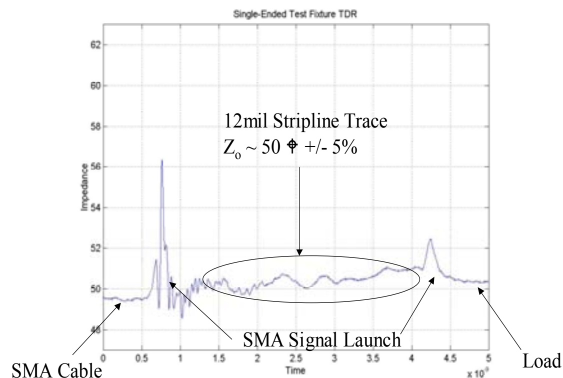

Figure 17. TDR measurements of test vehicle based on PTFE based composite and SMA

measurements show a modest deviation from 50 ohms with the SMA signal launch. S21 parameters were then measured using a network analyzer. The results are shown in Figures 18-20 for trace lengths 10, 20, and 30 inches. The PTFE based composites show a loss of 4 (10"), 7 (20"), and 11 db (30") respectively vs 8, 16, and 24 db for the analogous construction based on FR4. (This testing was deemed a necessity by Teradyne/Taconic to eliminate the influence of the FR4 daughtercards used in the previous signal integrity measurements.)

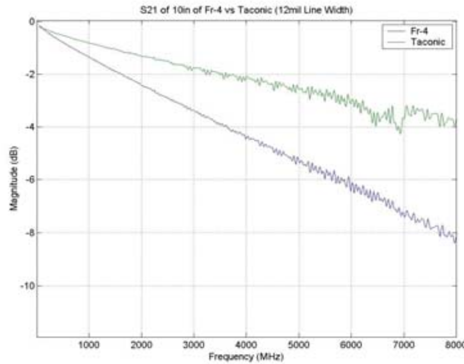

Figure 18. Loss in dB of PTFE based laminates vs. FR4 using a 10" trace in a stripline geometry.

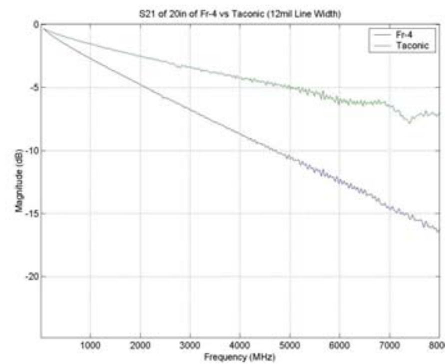

Figure 19. Loss in dB of PTFE based laminates vs. FR4 using a 20" trace in a stripline geometry.

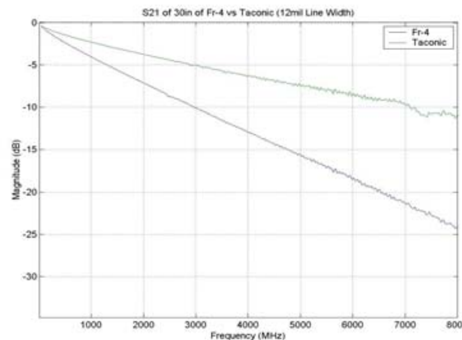

Figure 20. Loss in db of PTFE based laminates vs FR4 using a 30" trace in a stripline geometry.

This test vehicle was then used for signal integrity measurements in an analogous fashion as described in the earlier section on eye pattern measurements with the exception that NO DAUGHTERCARDS were used. The results are shown in Figures 21-23. At 2.5 Gbps neither FR4 or PTFE are seriously challenged. At 5.0 Gbps the PTFE based backpanel has roughly doubled the eye height. At 12.0 Gbps the eye is closed for FR4 while roughly 180 mV of eye opening is present for the PTFE based backpanel. This suggests that in the absence of any devices PTFE based backpanels should be able to support >10 Gbps in a properly designed system in the absence of any devices. The data further suggests that coupling PTFE with a device such as Gennum silicon, for example, should be able to extend the usefulness of copper based backpanels and interconnects well out into the future.

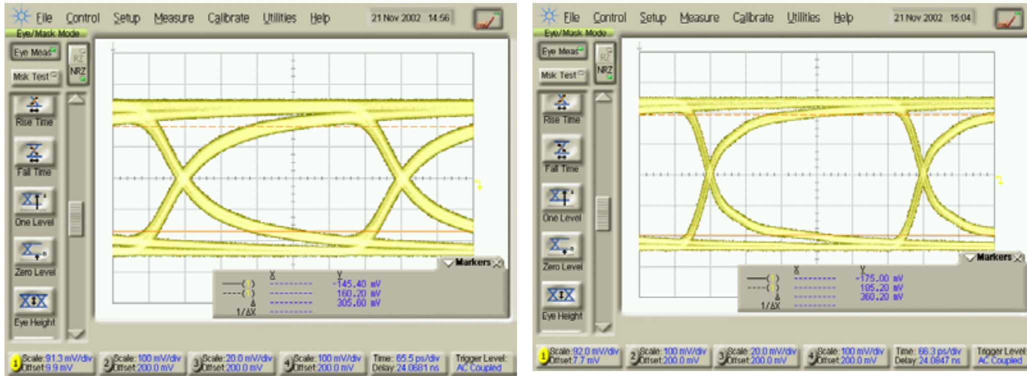

Figure 21. Signal integrity measurements of FR4 (left, 91 mV/div) vs PTFE (right, 92 mV/div) at 2.5 Gbps, 500 mV voltage swing (250 mV peak, 2^-23 PRBS), 20" trace length, 12 mil line width, launched directly onto the backpanel, no daughtercards, single ended.

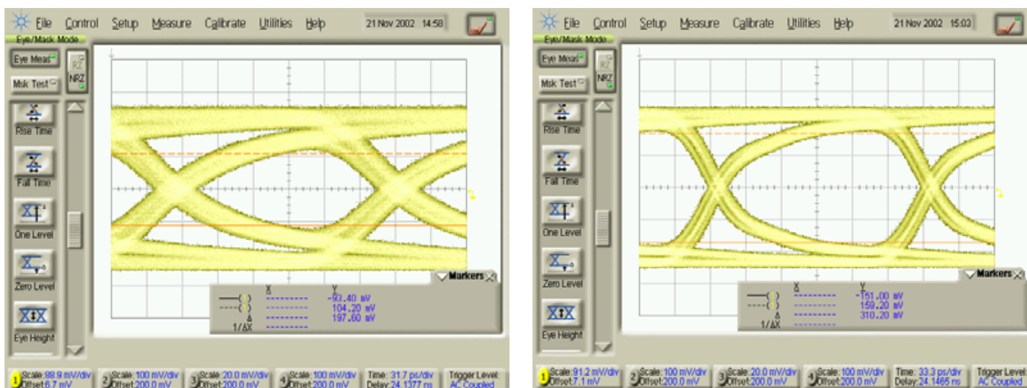

Figure 22. Signal integrity measurements of FR4 (left, 89 mV/div) vs PTFE (right, 91 mV/div) at 5.0 Gbps, 500 mV voltage swing (250 mV peak, 2^-23 PRBS), 20" trace length, 12 mil line width, launched directly onto the backpanel, no daughtercards, single ended.

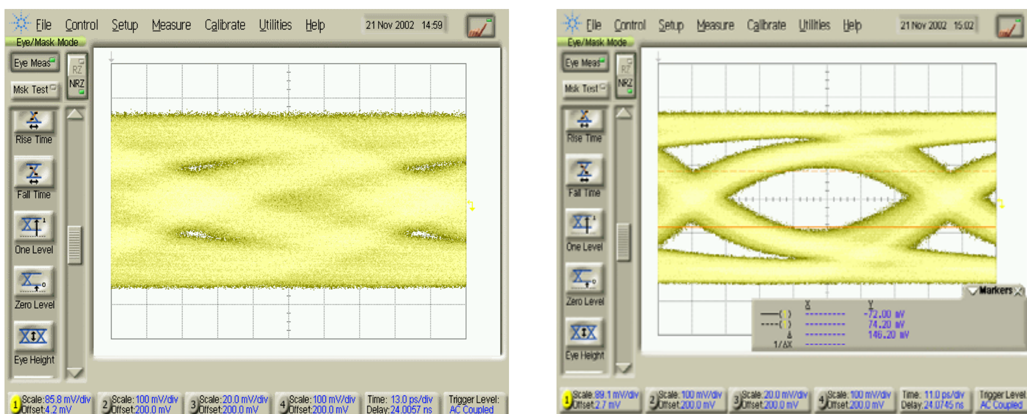

Figure 23. Signal integrity measurements of FR4 (left, 86 mV/div) vs PTFE (right, 89 mV/div) at 12.0 Gbps, 500 mV voltage swing (250 mV peak, 2^-23 PRBS), 20" trace length, 12 mil line width, launched directly onto the backpanel, no daughtercards, single ended.

Pricing

Pricing of the PTFE/fiberglass/adhesive hybrid takes advantage of the following key factors: (1) PTFE has become a commodity in recent years as it has been adopted by the telecommunication industry serving in various base station applications (2) the adhesive component of the composite is processed by a high volume FR4 laminator** (3) lay-up and lamination is carried out in a highly mechanized fashion by a world wide high volume FR4 laminator using a conventional FR4 cycle. Table 2 in Appendix A shows the cost multiple of the PTFE/fiberglass/adhesive vs standard FR4 for various scenarios. The direct material costs of a PWB is assumed to range in the best case of 30% to 35% of the PWB. The laminate and prepreg percentage of the direct materials is assumed to range from 55 to 70%. These are assumptions that are drawn from many layer multilayer PWBs and they are not intended to represent the actual costs of any given fabricator but should rather be considered ballpark numbers. Therefore, the direct laminate material costs are 16-25%. If a board is assumed to cost $0.075/in2 ($10.8/sq2) for all constructions and a multiple is attached to that based on a materials multiple over FR4, multiplied by the actual laminate material content percentage, a price for the material in question is obtained (Lam & Prepreg $/in2). If a constant fabrication cost is added (assuming one does not account for very high drill wear, for example for competitive materials, or the plasma activation of a PTFE plated through hole), the total cost to fabricate the PWB is calculated. Dividing that number by the baseline cost to manufacture an FR4 PWB yields the cost multiple of the material in question over FR4. The PTFE/fiberglass/adhesive laminate multiple is based on current quoted product relative to the pricing of FR4. The number is adjusted according to the volumes in questions. Therefore, a multiple of 1.6 (best case) to 1.9 (worst case) over FR4 is expected for a finished PWB using the PTFE/fiberglass/adhesive composite.

Conclusions

PTFE material offers signal integrity up to 12.0 Gbps in the absence of any devices to improve signal integrity. Research to date suggests that PTFE is robust enough to offer good thermal reliability and can be readily fabricated into a high layer count backpanel. The unanswered question is…at what point does a finished board containing PTFE that costs 1.6 to 1.9 x FR4 become the preferred approach to reaching 10-12 gbps over alternative solutions?

*RF35P, a low loss PTFE/fiberglass RF product from Taconic
**TacLam™ 3200/IS630, PTFE/fiberglass/adhesive based cores from Taconic and Isola AG

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[2] Grasser, Eduard, and Katzier, Helmut, "Kuenftige Anforderungen von Telekommunikationssystemen an die Verbindungstechnik", 5th Ruwel Symposium, June 13-14, 2002.

[3] Kataoka, Takashi, "Copper Foil Technology for High Frequency Applications", **Proceedings of the IPC Annual Meeting**, New Orleans, November 3, 2002, S07-1-1.

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[5]Polymer Handbook
[6]White, S. R., Mather, P. T., Smith, M. J., "Characterization of the Cure-State of DGEBA-DDS Epoxy Using Ultrasonic, Dynamic Mechanical, and Thermal Probes", Polymer Engineering and Science, Jan. 2002, 42 (1), 59.
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[8]Aklonis, J. J. and MacKnight, W. J., Introduction to Polymer Viscoelasticity, John Wiley & Sons, 1983, 40-43.

Appendix A

Table 1. Laminate Properties of PTFE/fiberglass/adhesive

Property	Units	Typical Value	Method
Dielectric Constant (1 MHz, 15-35% resin)		3.20	IPC-TM 650 2.5.5
Dielectric Constant (10 GHz, 15-35% resin)		3.19	Bereskin[1]
Dissipation Factor (1 MHz, 15% resin)		0.0022	IPC-TM 650 2.5.5.5
Dissipation Factor (14.5 GHz, 15% adhesive)		0.004	Bereskin[1]
Dissipation Factor (14.5 GHz, 35% adhesive)		0.004-.005	Bereskin[1]
Peel Strength (warp) 0.5 oz reverse treated foil	lbs	5.6	IPC-TM 2.4.8
Peel Strength (fill) 0.5 oz reverse treated foil	lbs	6.4	IPC-TM 2.4.8
Moisture Absorption	(%)	0.1	IPC-TM 650 2.6.2.1
T260/T288/T300	min	>600/>60/>30	IPC-TM-650 2.4.24.1
PTFE:Epoxy ratio		5:1	
Glass Transition (PTFE)	(°C)	Room Temperature	(TMA)
Glass Transition (BT-epoxy)	(°C)	Non-detectable 128, 177 150-160	(DSC) (DMA) (TMA)
Resin Flow (15% adhesive)	(%)	0.5-1.0	IPC – TM 650 2.3.17
Resin Flow (25% adhesive)	(%)	6.0-7.0	IPC – TM 650 2.3.17
Resin Flow (35% adhesive)	(%)	10-14.0	IPC – TM 650 2.3.17
UL ratings		In progress	

[1] (Bereskin Patents 5,083,088 and 5,187,443)

Table 2. Cost multiple over FR4 for a finished board using PTFE based solution

BEST CASE	Relative cost of Material vs FR4	PWB Typical Total DM	Lam & Prepreg % od total DM	Total DM cost of lam & Prepreg	Board Cost. $/in 2	Lam & Prepreg $/in 2	Other PWB costs	Total Cost to Produce	Pwb Price X FR4	Mat'l % of PWB cost
FR4	1	0.3	0.55	0.165	0.075	0.012	0.063	0.075	1.0	0.17
Tacpreg/IS630 (volume)	4.5	0.3	0.55	0.165	0.075	0.056	0.063	0.119	1.6	0.47
Tacpreg/IS630 (medium volume)	5.5	0.3	0.55	0.165	0.075	0.068	0.063	0.131	1.7	0.52
TacPreg/IS630 (specialty)	7	0.3	0.55	0.165	0.075	0.087	0.063	0.150	2.0	0.58

WORST CASE										
FR4	1	0.35	0.7	0.245	0.075	0.018	0.057	0.075	1.0	0.25
Tacpreg/IS630 (volume)	4.5	0.35	0.7	0.245	0.075	0.083	0.057	0.140	1.9	0.59
Tacpreg/IS630 (medium volume)	5.5	0.35	0.7	0.245	0.075	0.101	0.057	0.158	2.1	0.64
TacPreg/IS630 (specialty)	7	0.35	0.7	0.245	0.075	0.129	0.057	0.186	2.5	0.69

Appendix B

Figure 1. Test Setup for Signal Integrity Measurements

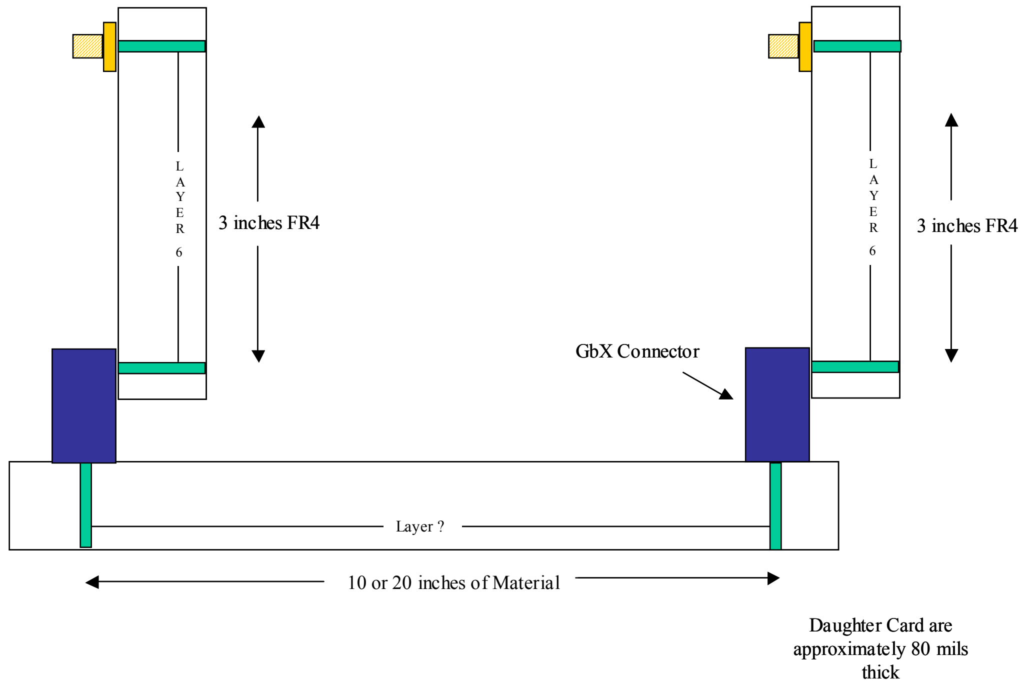

Figure 2. TDR measurements of 20 layer backpanel used for signal integrity measurements