

Thin Dielectrics in PWB Techniques And its possibilities for DCA and High Density Applications

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Abstract

By introducing thin dielectrics new possibilities have been opened for the electronic packaging and interconnection. Thin dielectrics have made it possible to produce small holes and still assure controlled plating. But there has been also been opening more possibilities; photo via technology is more photo dielectric, which makes it possible to attach different kind of dielectrics were you want to have it on the board. Even more: the thin dielectrics are mostly unreinforced, which means that the thin layers are floating on the rigid centre carrier, which also opens new possibilities.

All these possibilities must result in a question: Where are we going? What are our ultimate goals?

Buried chips will make denser packaging and Offset printing opens a fully depositing technology with fewer waste products.

The PWB-industry is certainly facing an interesting future.

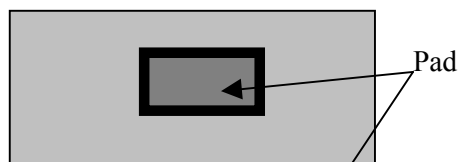
Laser via or Photo via?

The question “laser via or photo via ?” is often mentioned. The answer is that it is “Both!” It depends what you want to do.

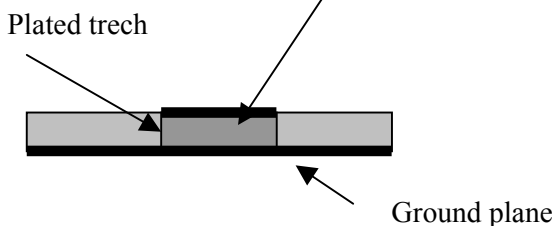
The drive force to introduce these two mentioned technologies were to get smaller vias than you can get with conventional drilling.

But you can also do much more with the technology as shielded conductors and low impedance ground pads by making trenches around the edge of the pad and then plate it:

Top view:

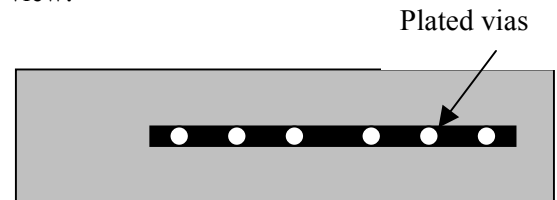


Side view:

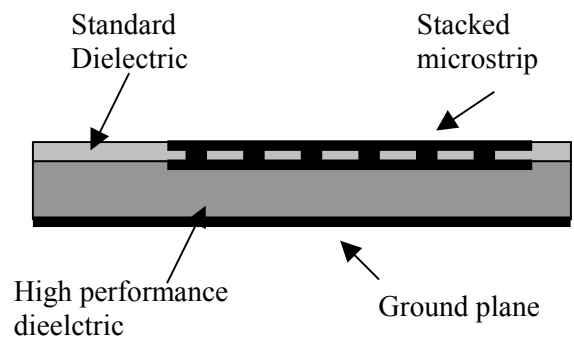


An another possibility is to “lift” a better dielectric’s performance from a inner layer to a surface layer by “stacked microstrip”.

Top view:



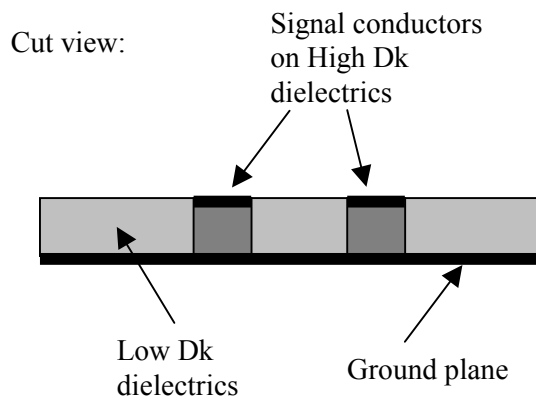
Side view:



The Photo via technology opens more possibilities; here the question is more:

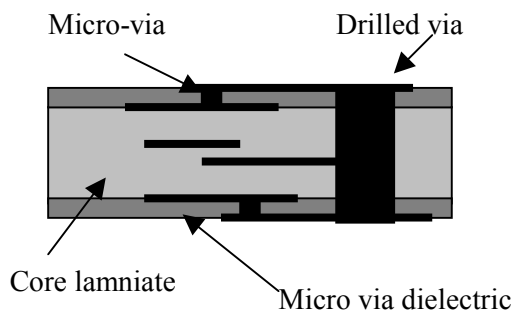
Photo via or Photo dielectric ?

In the photo via technology you have possibility to develop the areas you want to use. Most common is just to develop holes but there are certainly more possibilities. A major problem with denser pattern in more compact electronics is crosstalk. Shielded conductors are a possibility. Another is to put a higher dielectric just under the conductor which will bound the field to the ground plane.



Floating Dielectrics

If we look on a typical PWB for cellular phones today many of the boards will look like:



Independently if the micro via dielectric is Resin Coated foil or some photo dielectric it is mostly unreinforced material laminated on a rigid core. The rigid core will take care of the most of the mechanical properties of the board. This means also that with more micro via layers at the top surfaces you can move the most of the electrical properties to the top layers. Normal glass-epoxy laminate has a CTE of some 16-18 ppm/C, which is not so good conditions

for Flip-Chip and CSP. The reason is the low glass content in the laminate; mostly around 50%. If we increase the glass content to some 75 % the CTE will go down to around 9-10 ppm/C, which is much better.

Thin PTFE-substrates

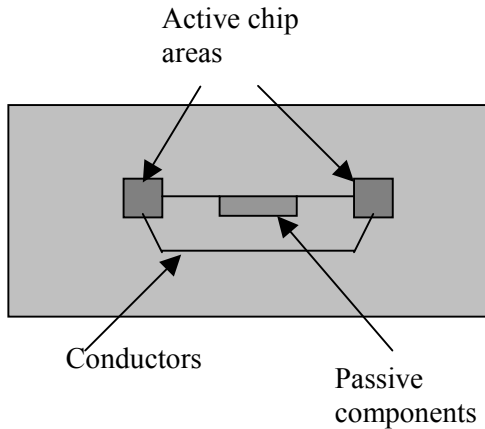
Ultra-thin PTFE is also possible to use as microvia-substrate with a floating capability on a rigid carrier. The Rogers 3000-series are possible to get down to at least 62 μm and TACONIC TAC-LAM down to 50 μm .

An interesting observation after has working with these materials is that if used in right way no chemistry as "Tetra-etch" is needed. The rough surfaces on the laser-drilled holes seem to give enough adhesion of copper. The lamination could be done with epoxy pre-pregs under at least three conditions:

- Lamination on PTFE-materials with high ceramic contents will give adhesion to the ceramic content.
- In a microstrip design on the top-layer it is possible to have dominating ground plane of copper which takes care of the adhesion.
- If electro-deposit copper (ED-copper) is used; the "foot-print" of the copper and its treatment will be on the PTFE-surface a number of hour after the etching if it is carefully treated. This surface will give a good adhesion to the epoxy pre-pregs at some laminates.

Were we going?

To understand that it is important to have a vision of a model for an "ultimate" concept. If chip-area was very cheap and with reasonable good mechanical properties, we should have used chip-material as PCB and make interconnections on it and even solder passive components on it. This carrier should also have to meet every needed chip technology, even as GaAs etc. A "Multi-chip-technology wafer" to very low cost.



If this was possible we could forget all:

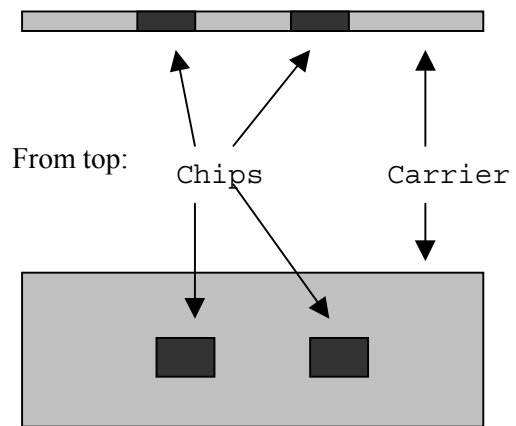
- Problems with electrical connections between chip and carrier, because they are made on the same media.
- Problems with mechanical miss-match between chip and carrier.

At the same time we have got a chip-thin carrier with integrated chip. This is quite ultimate. Now chip-area is not very low-cost, and we need different types of chip technology on the same carrier, and after all chip-area is not so good as chip-carrier. But now we have a vision. Let's try to get it.

Chip-Thick Carrier

As it is hard to have a total chip-area over the total carrier. Let's implement a chip-thick chip-compatible carrier. This material should have CTE corresponding to the actual used chip-technology, good mechanical properties and good thermal conductivity. With this material it is possible to make holes for the chip which are in close tolerances to the actual chip-sizes. Examples for this type of materials are AlSi and AlSiC. Others are possible as LTCC-based materials. The carrier could be copper-plated to get a proper ground-plane.

Chip-thick carrier from side:

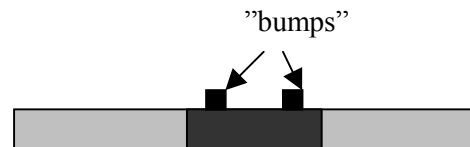


The attachment of chips could either be done on a thin flexible metal-foil, which covers the bottom of the chip-cavities and the total bottom-side of the carrier. Or the chips could be temporary attached during this step and finally attached during the operation "Buried bump".

Buried Bump

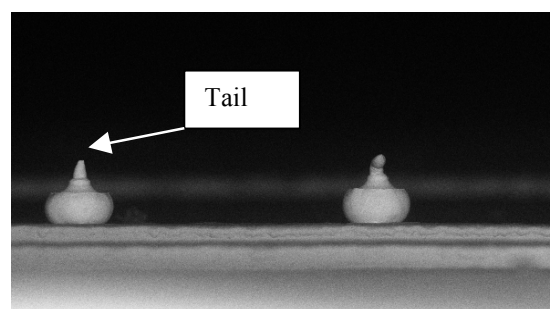
The connection-areas on the chips; "bond-pads" can be prepared with "bumps" as final operation at the chip supplier before they are cut out from the wafer.

Chips with bumps with carrier; side view:



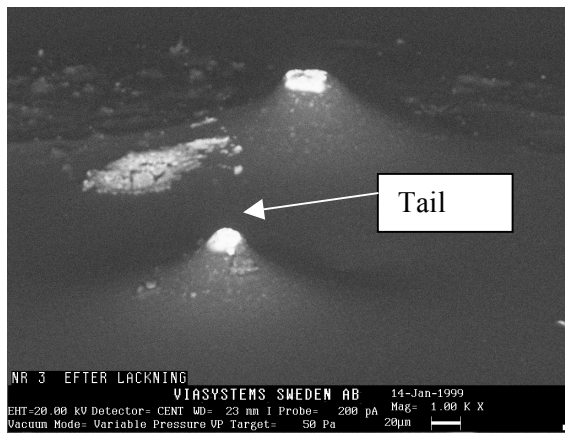
In our tests we have used "ball-bumps", however plated bumps in the wafer-process is to prefer. By using bumped chips, which pass the dielectric, it is possible to meet the bumps with quite big connection-pads. The most often described method to connect the chip with laser-vias will give bigger problem to find and hit the small bondpads on the chip

Photo of ball-bumps of wire:

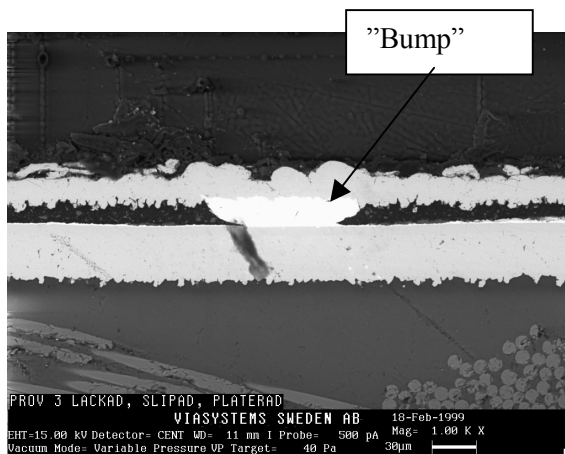


Next step is to cover the carrier with liquid dielectric.

Ball-bumps covered of lacquer:



After wet grinding (to much in this case) and plating:



This will give direct-connected conductors without soldering or conductive adhesions. At least one more SBU-layer with conductors could be applied. As the core carrier will have a chip-compatible CTE it is possible to attach a Flip-Chip anywhere on surface.

The possibilities with Offset printing.

The most ideal component carrier will have to meet the same performance of pattern dimensions as the chips they have to interconnect. This to reduce the problems with "fan-out" from the chips.

This will result of conductors down to some 5 um or smaller.

Matching thickness of dielectrics for these conductors will be some 5 - 15 um and via-connections between layers down to some 10 - 30 um.

There is a need to bury or integrate more passive electrical components in the pattern of the PWB. This to lift out passive functions from the chips.

We have earlier mentioned the problems with cross-talk between different conductors and to have different electrical performances at different parts of the PWB.

The present PWB technology has hard to meet the demands mentioned above.

Added to that the present PWB-technology is not an environmental friendly concept. We are etching away nearly more copper than is on the final board. A multilayerboard has a numberless development and stripping operations of photo-resist and solder-resists.

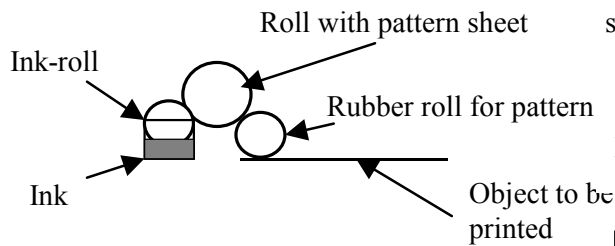
Offset printing is a fully depositing method, all material used will be on the final product. The accuracy is in the range we need.



Fig. A complete bible printed on one poster. Standard offset printing with distinct letters made of "track-width" 25 um.

The limitation to introduce offset printing as a pattern-transfer method has been the low conductive inks based on silver or carbon. Reports of conductive polymers are coming but still not commercial. During the time is possible to use offset printed polymer activators as a pre operation for chemical copper.

If we look at the fundamentals of offset printing:



Several types of inks is possible to print in one line by arrange several printing station after each other in one line. Four to six stations are common, but more is possible.

The accuracy of the offset printing process is in the range of future demands for PWB's.

The method to reach that - an incremental on-the-spot concept for every point on the surface - is very interesting to learn for the electronic industry.

The offset printing process is a fully depositing method, which means that nearly the only used material will be found on the final product.

The offset printing method has a mass-capability production profile, which is interesting to study for the electronic industry.

Offset printing adapted to manufacturing of PWB

The idea here is to adapt the component carrier technology as much as possible to the present infrastructure of printing techniques, which means to work with flexible materials. This is not a big suffer as many PWB's are flexible and even sheets in rigid boards are flexible before they are laminated.

The most modern printers are today mostly working with flexible materials, however there are machines for more rigid materials.

Offset-printing are mostly maintained in lines were several inks are printed sequentially after each other: E.g. colour-prints are printed are printed in a four-ink printer; red, blue, yellow and black. This is done with very high accuracy to get a perfect picture.

Sequentially printing suits very well for electronic PWB.

It is possible to print dielectric between the conductors (which will form the conductors) in the same line as the ink for the activator is

printed. The activator will later show the electroless plating bath were the solid metal should be plated.

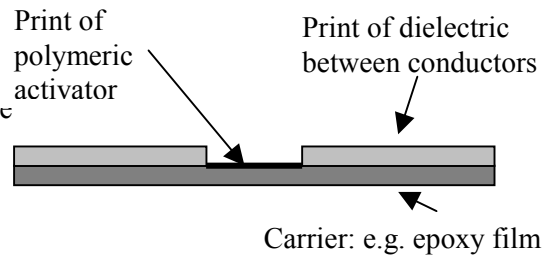
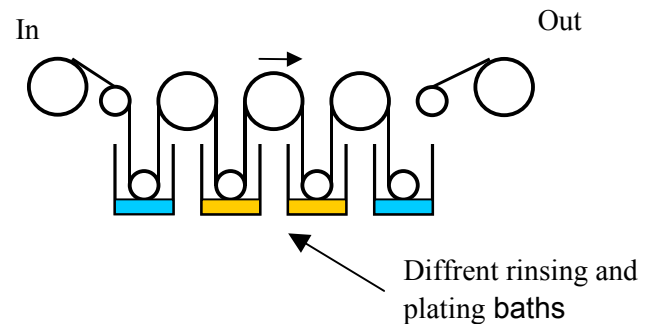
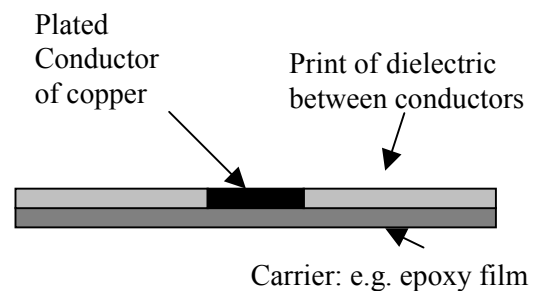


Fig. Printing of activator and dielectric

Next step could be electroless copper-plating in a roll-to-roll process



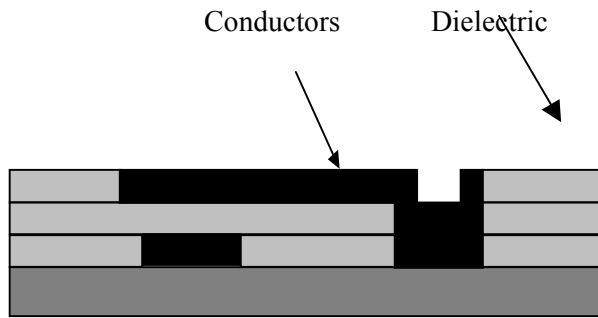
After plating the result will be:



If more layers are requested next printing operations could be:

- Dielectric between layers
- Activator for next layer of conductors
- Dielectric between conductors

All in one three-ink printer:



Future possibilities

A first project should mainly convert some present PWB's and not test all possible advantages with a multiple print process with several types of inks, But some possibilities should here been pointed out:

Print of resistors

The present screen-printing process to print resistors are maintained by extra operations and mostly with low tolerances concerning resistor values – often approx. 20% – therefore seldom used.

The offset printing method are more exactly in thickness and to control size of printed areas. Added to that: possibilities to use several types of inks in the same printing operation will help get more resistor values.

Printing of polymeric semiconductors

We are just in the beginning of an evolution of polymeric semiconductors.

Examples of that is polymer light emitting diodes which could be found at:

<http://www.iap.fhg.de/public/ag33/device1.htm>

Offset printing is a technology that can meet this, which the present PWB can not.

Printing of polymeric non-metal conductors

Here we are just in the beginning of an evolution.

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